

HDI PCB manufacturing process

AGENDA

1. Detail Manufacturing

4-65

- ***Process Flow (Photo)***
- ***HDI Products***

2. Technology Roadmap for PCB & HDI

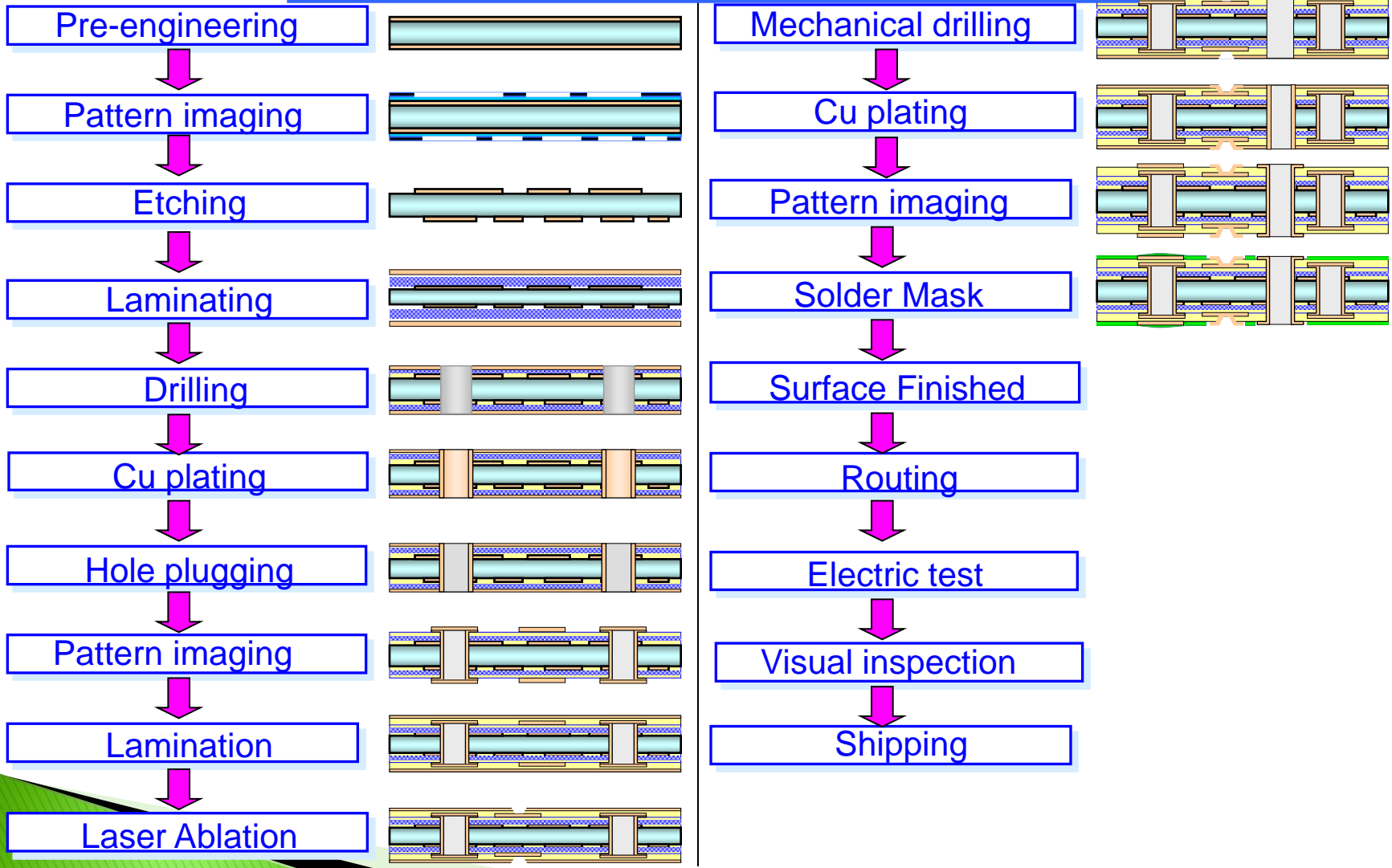
66-70

- ***Technology Roadmap***
- ***Process Capability***

Process Flow

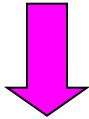
(PCB&HDI)

Process Flow Chart (1)

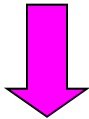


Process Flow Chart (2)

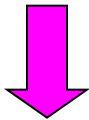
Pre-engineering



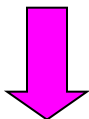
Pattern imaging



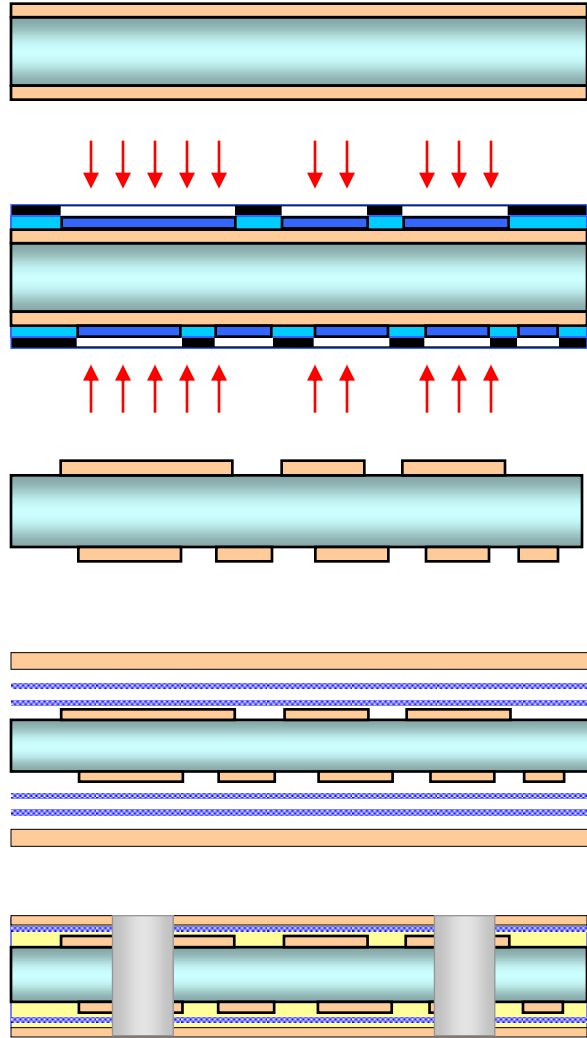
Etching



Laminating

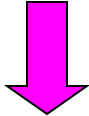


Drilling

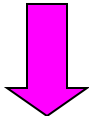


Process Flow Chart (3)

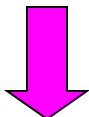
Desmear



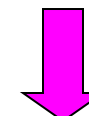
Cu plating



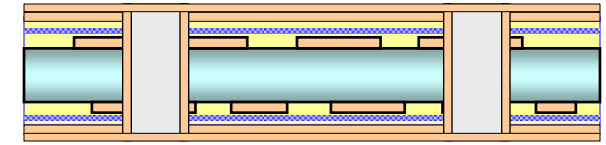
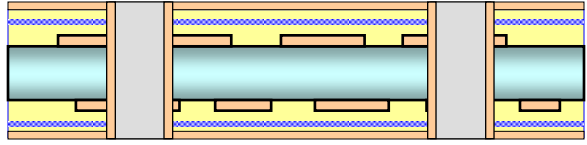
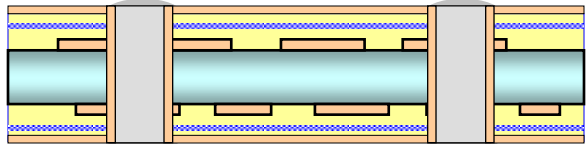
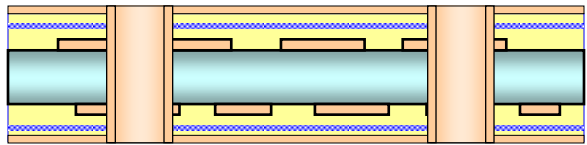
Hole plugging



Belt Sanding

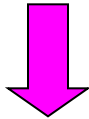


Cu plating

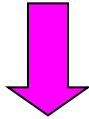


Process Flow Chart (4)

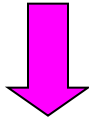
Pattern imaging



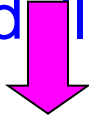
Lamination



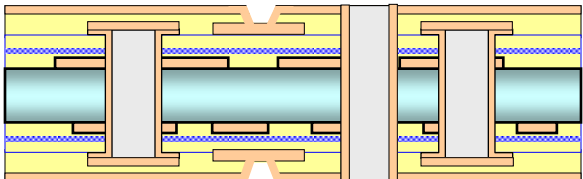
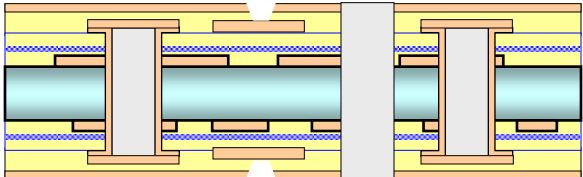
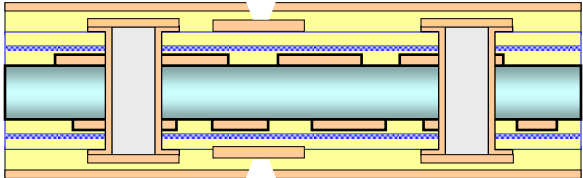
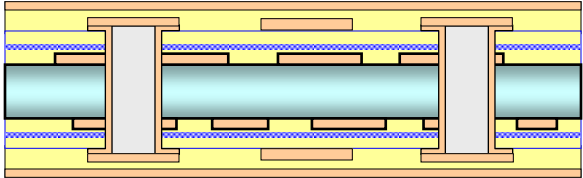
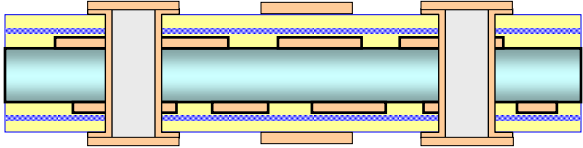
Laser Ablation



Mechanical
drilling

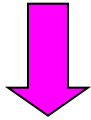


Cu plating

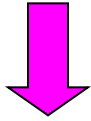


Process Flow Chart (5)

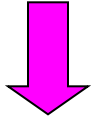
Pattern imaging



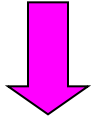
Solder Mask



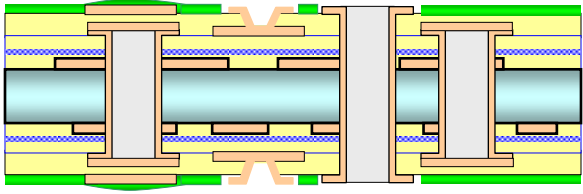
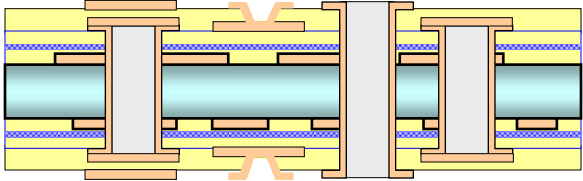
Gold plating



Routing

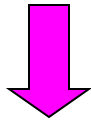


Electrical test

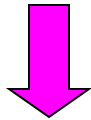


Process Flow Chart (6)

Visual inspection

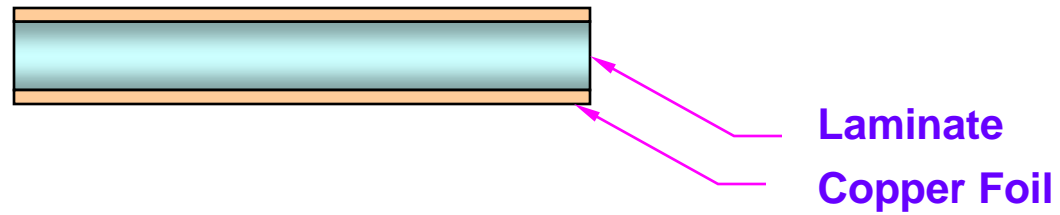


Hole counter

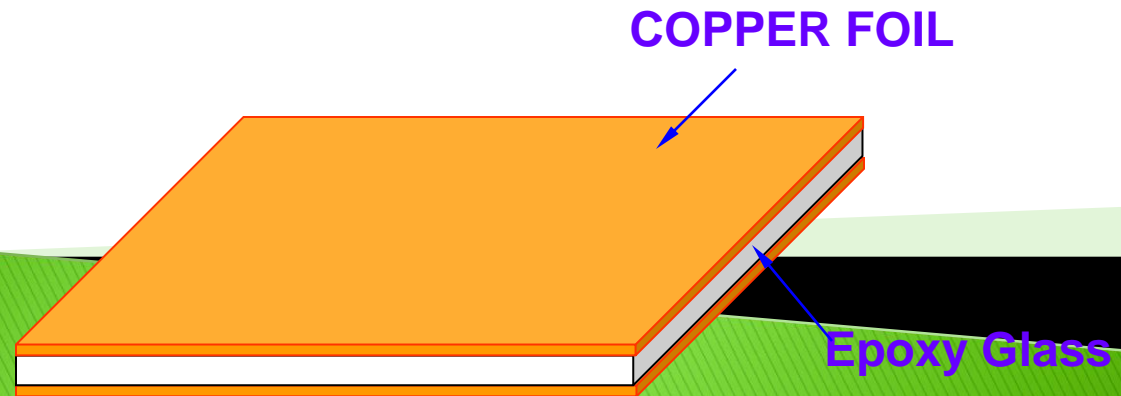


Shipping

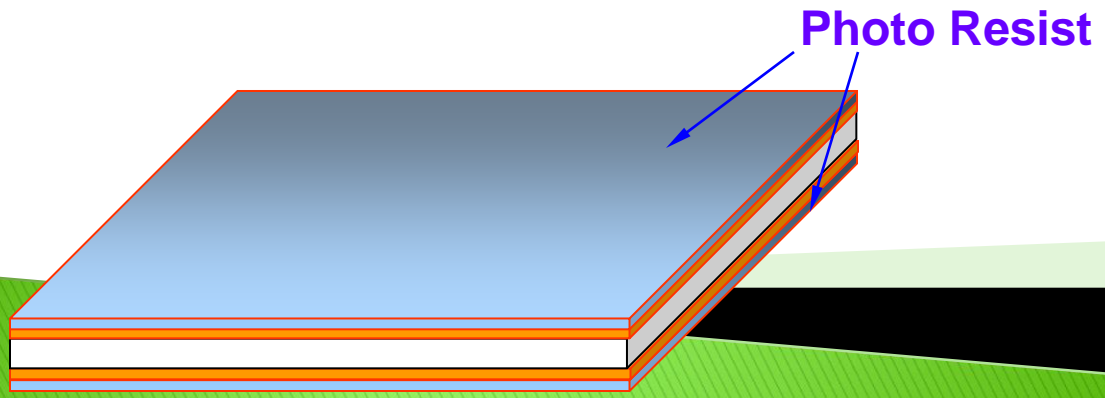
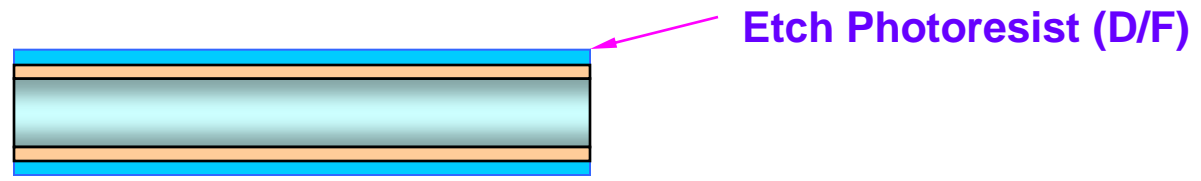
1.內層基板 (THIN CORE)



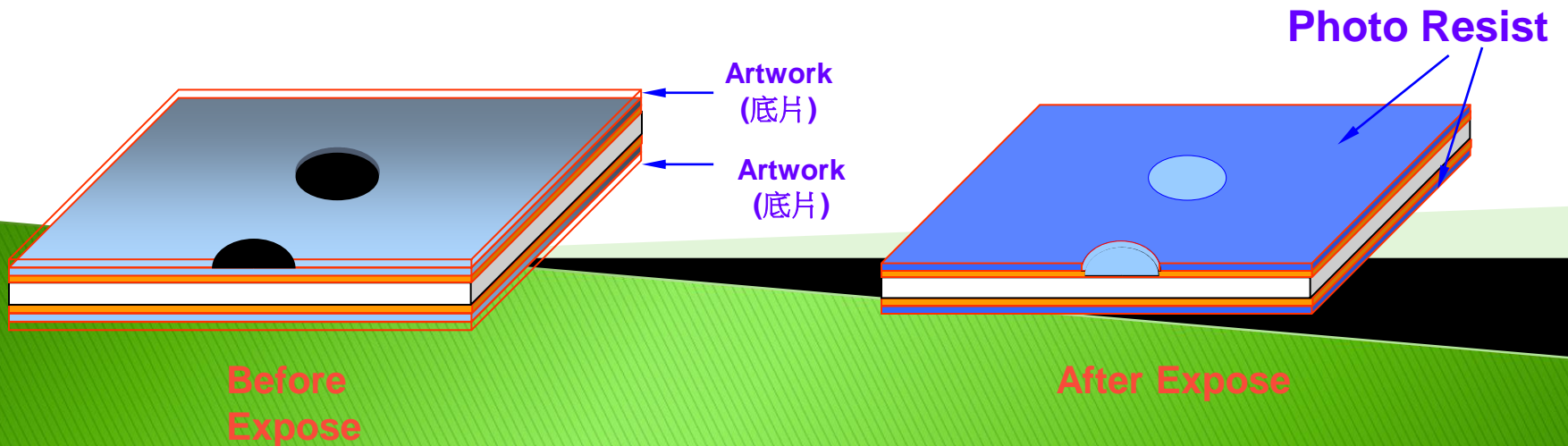
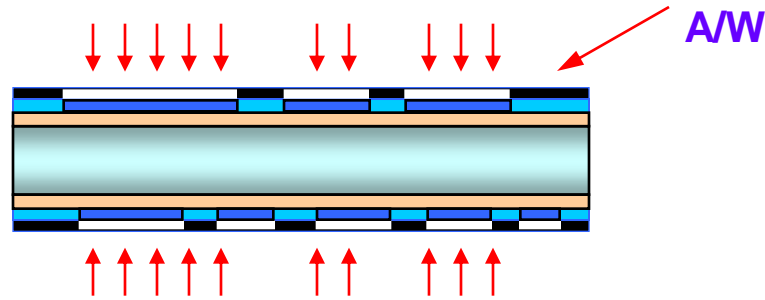
裁板 (Panel Size)



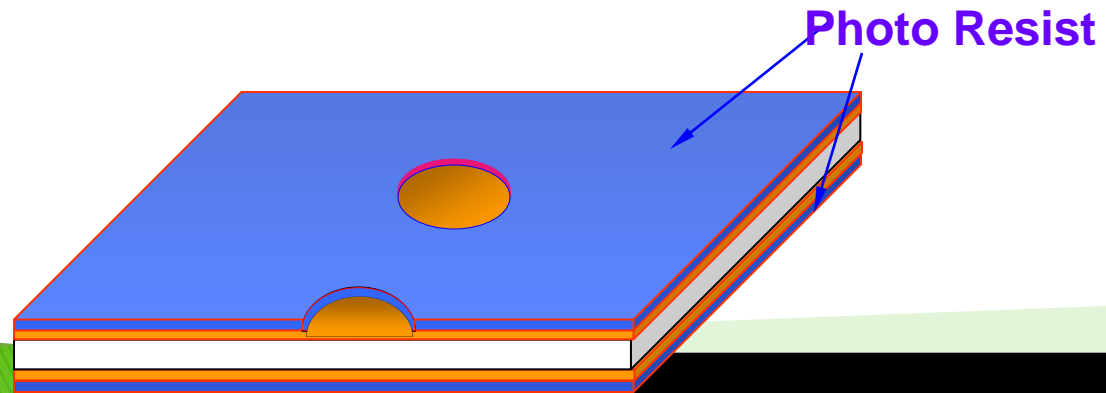
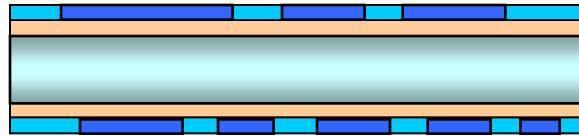
2.內層線路製作(壓膜) (Dry Film Resist Coat)



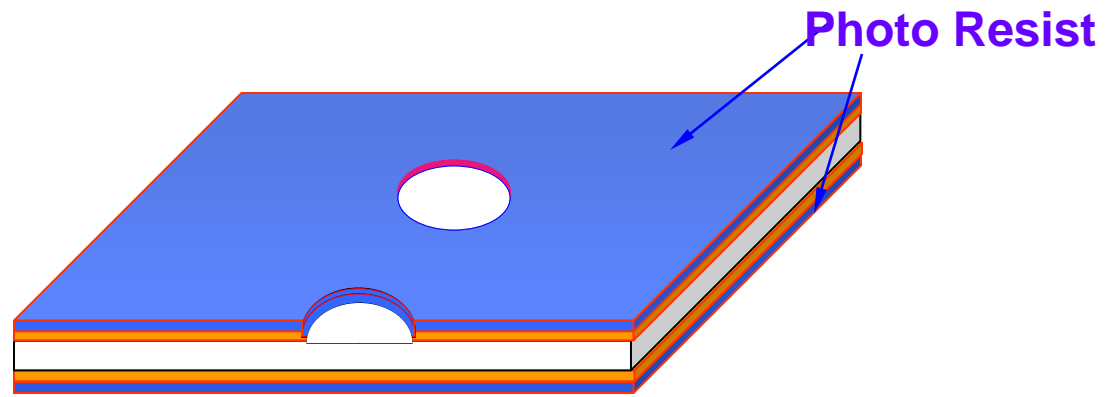
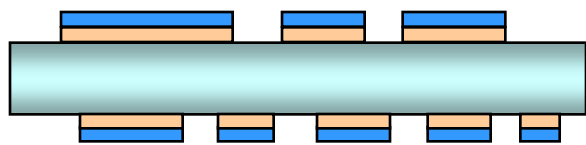
3. 內層線路製作(曝光)(Expose)



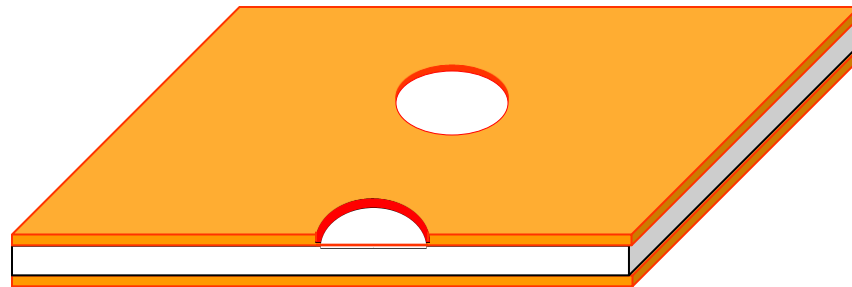
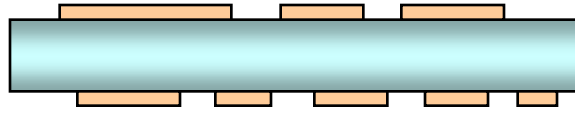
4. 內層線路製作(顯影)(Develop)



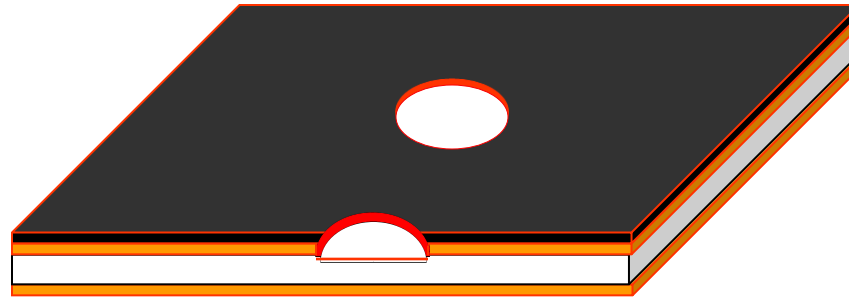
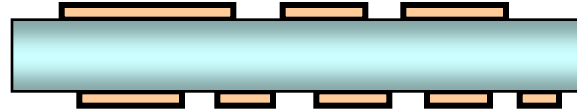
5. 內層線路製作(蝕刻)(Etch)



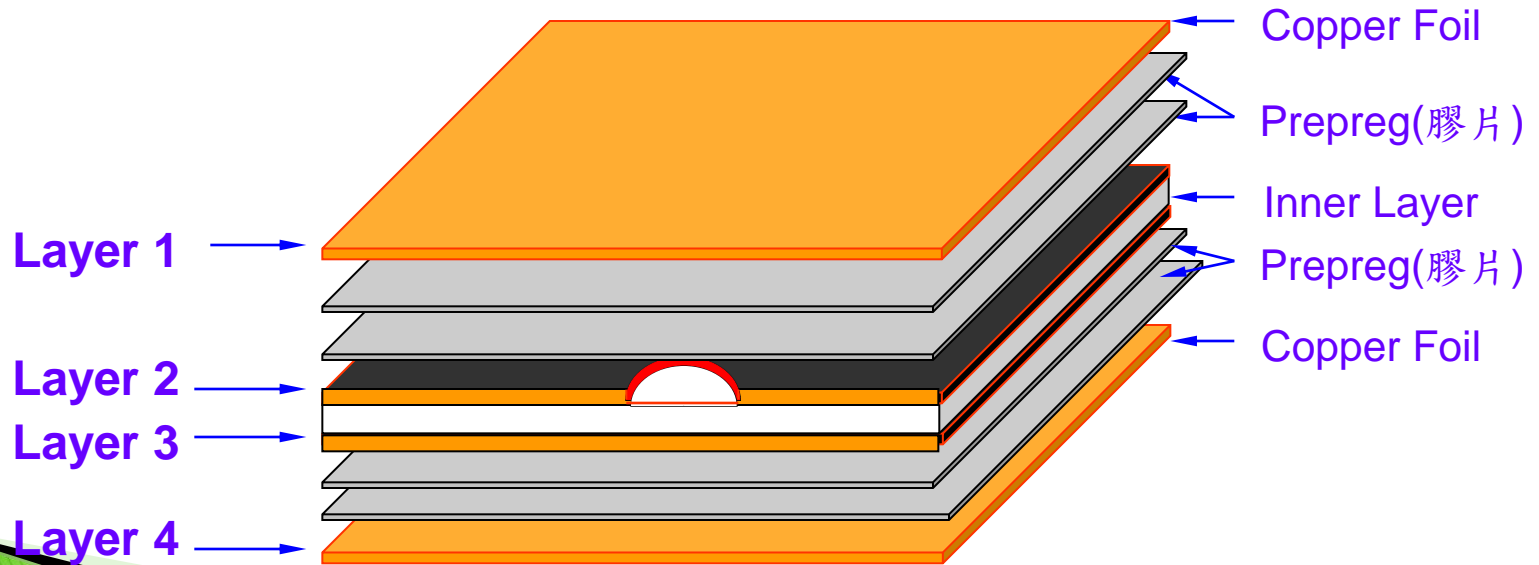
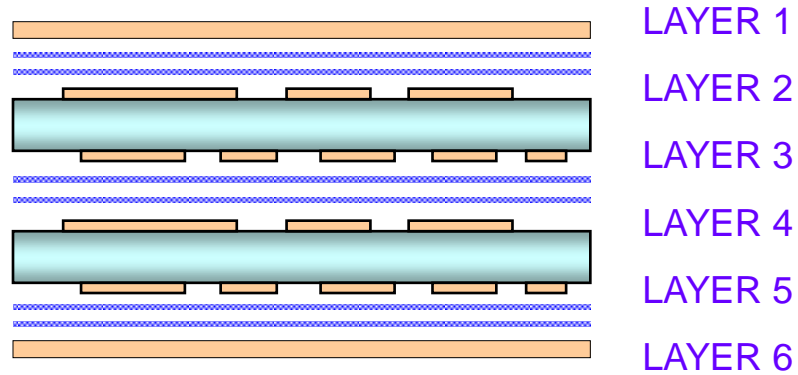
6. 內層線路製作(去膜)(Strip Resist)



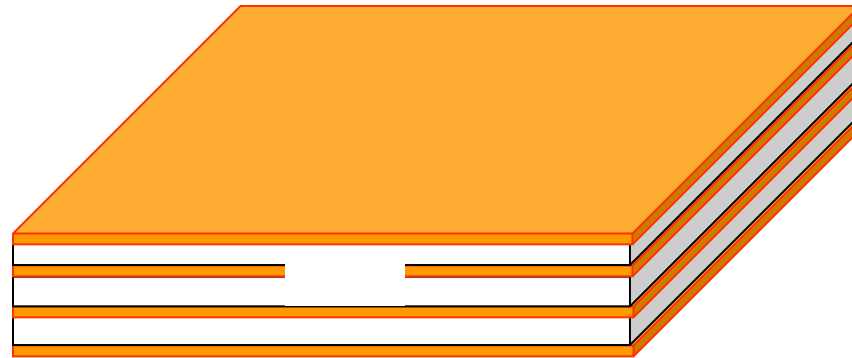
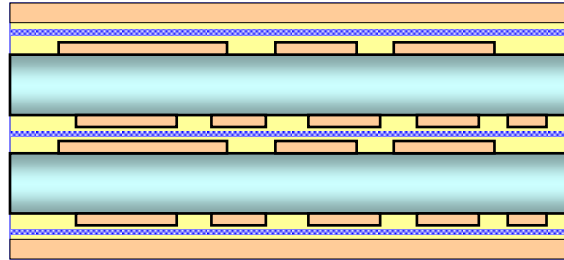
7. 黑氧化 (Oxide Coating)



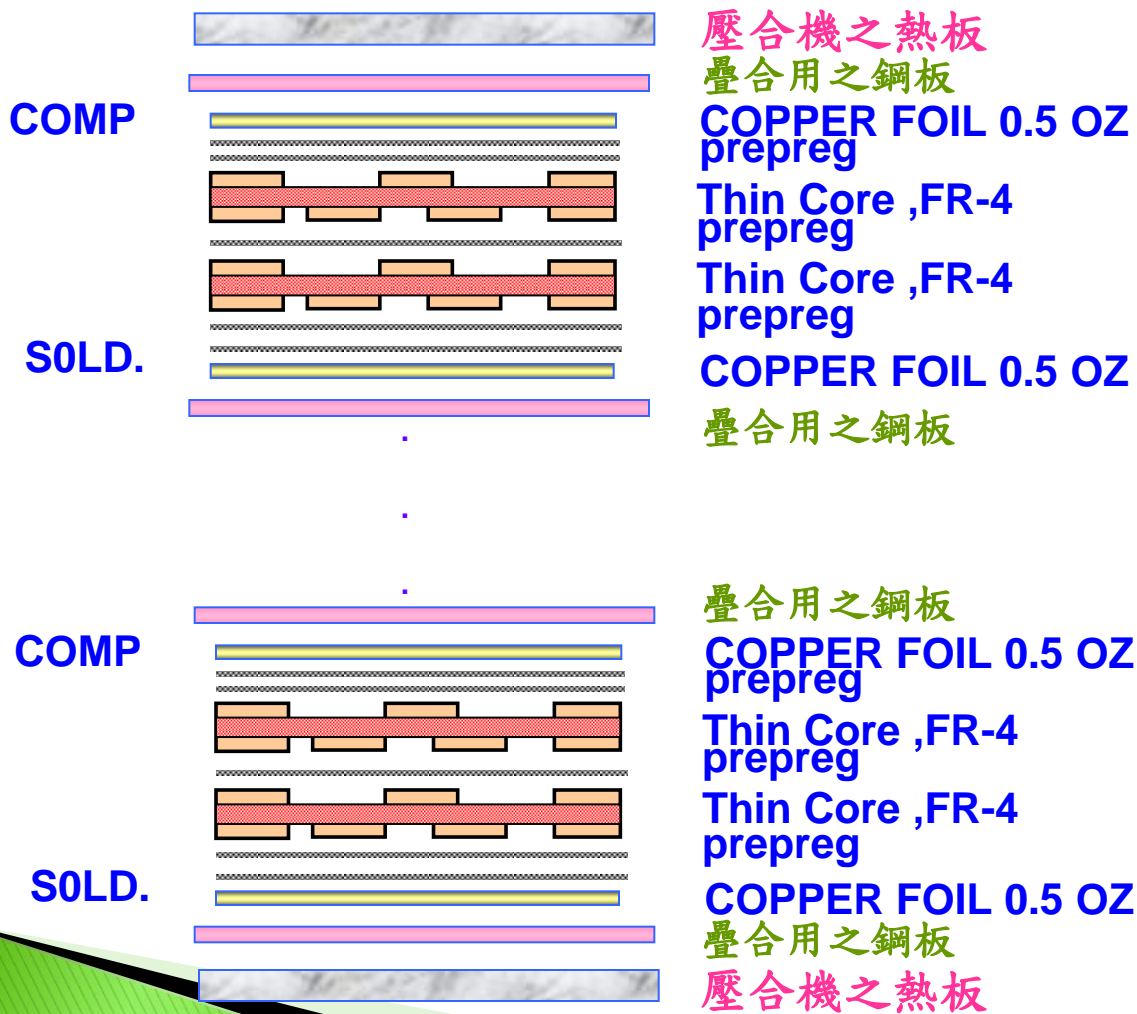
8. 疊板 (Lay-up)



9. 壓合 (Lamination)

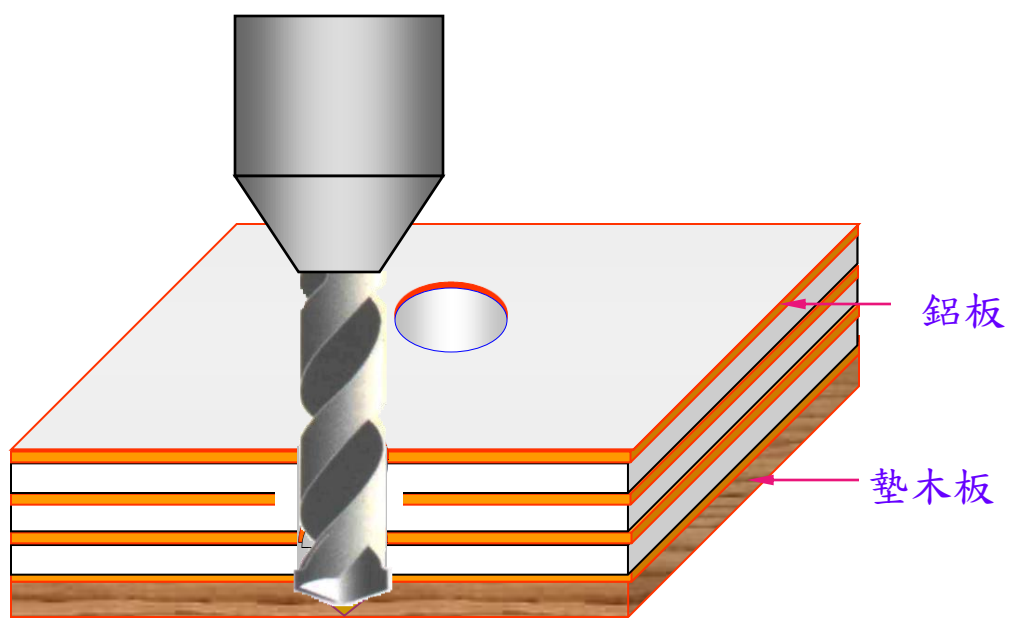
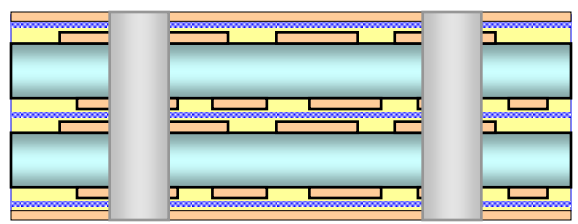


典型之多層板疊板及壓合結構

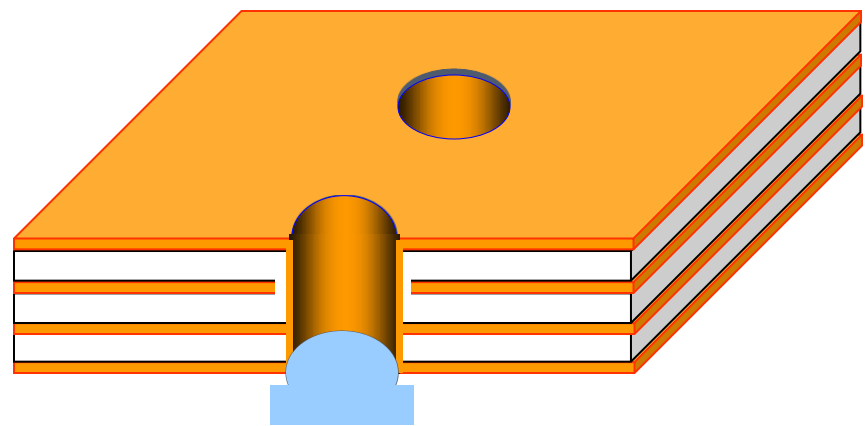
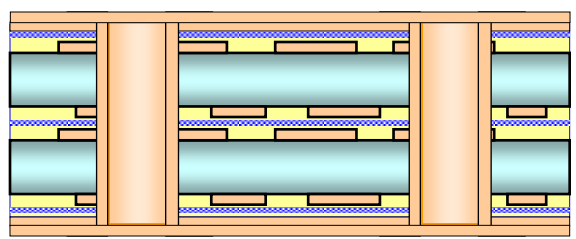


10-12層疊合

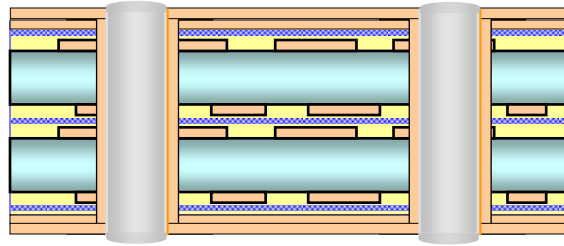
10. 鑽孔 (Drilling)



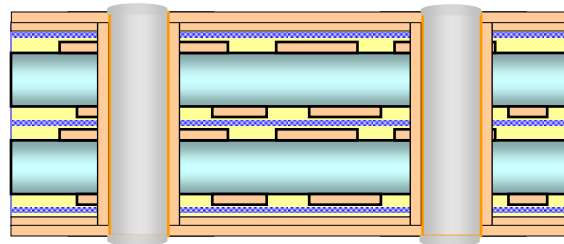
11. 電鍍Desmear & Copper Deposition



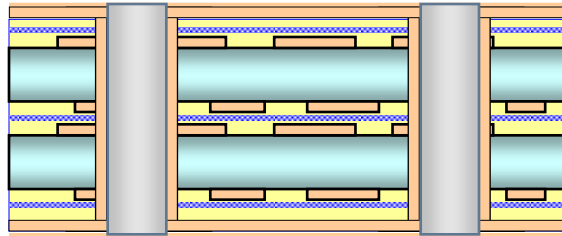
12. 塞孔(Hole Plugging)



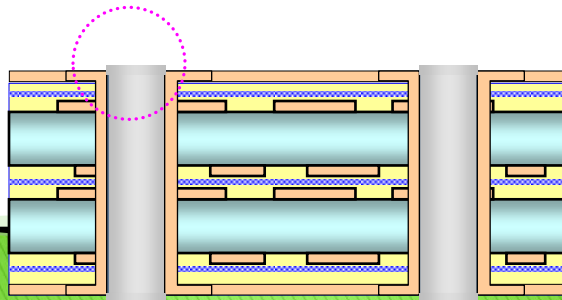
13. 去溢膠 (Belt Sanding)



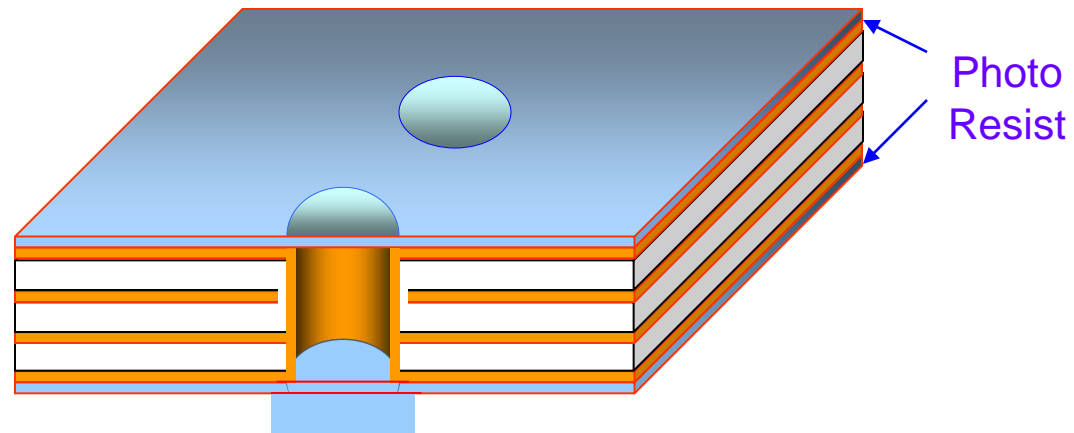
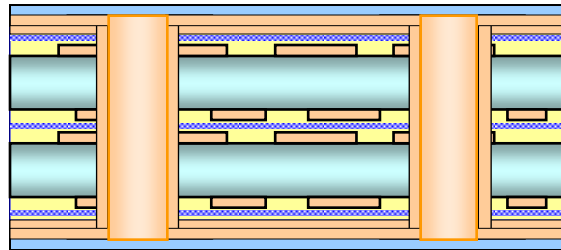
14. 減銅 (Copper Reduction) → Option



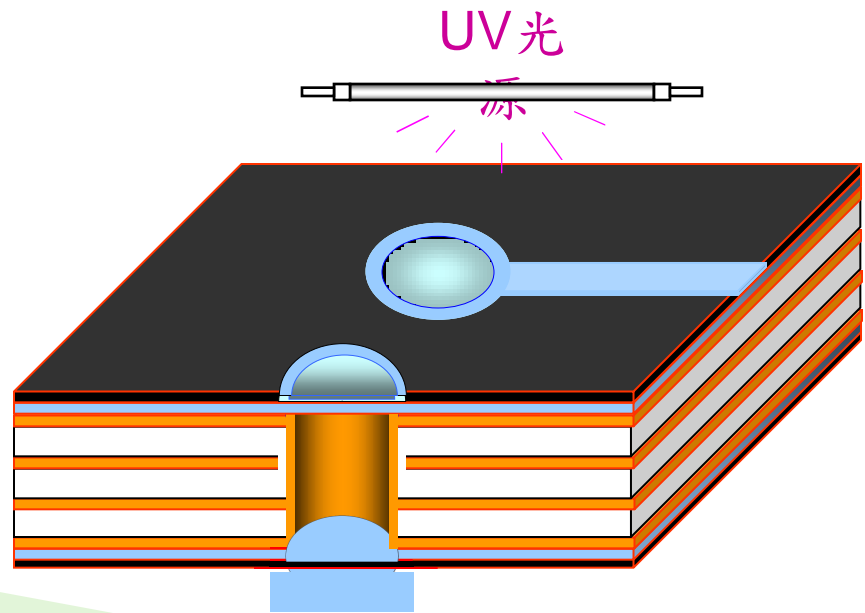
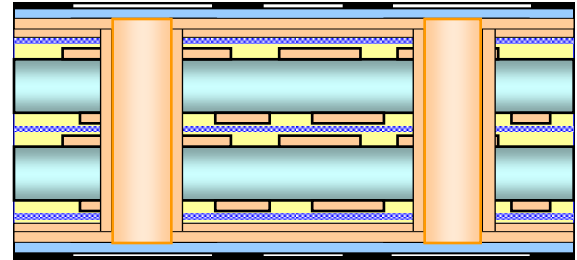
15. 去溢膠 (Belt Sanding) → Option



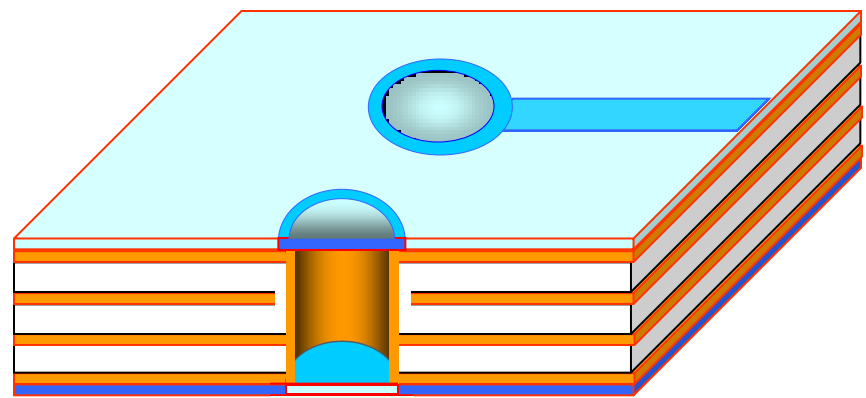
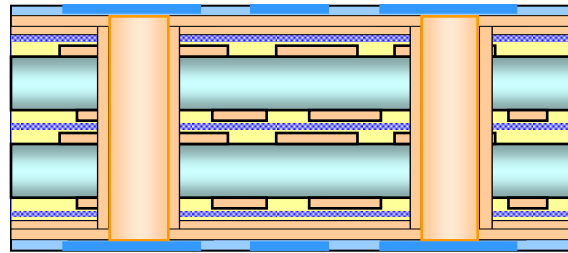
16. 外層壓膜 Dry Film Lamination (Outer layer)



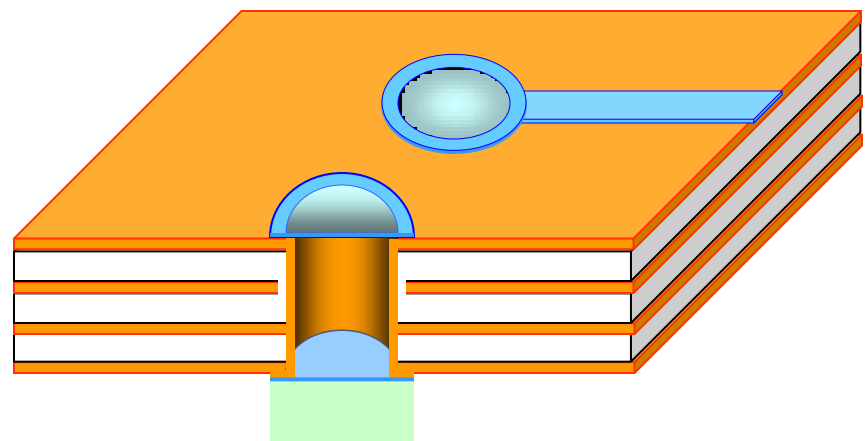
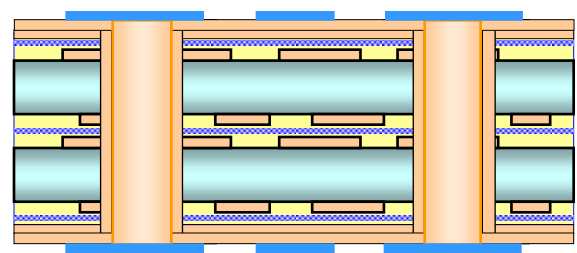
17. 外層曝光 Expose



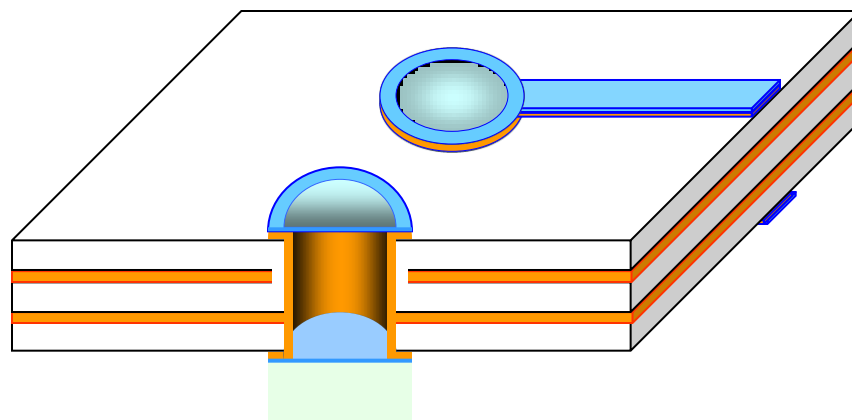
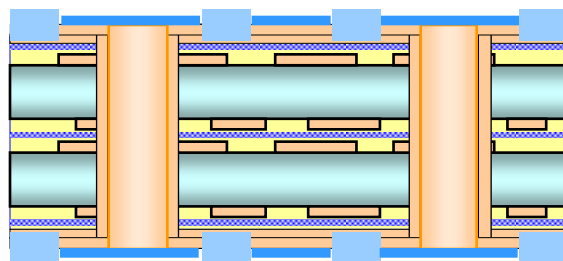
18. After Exposed



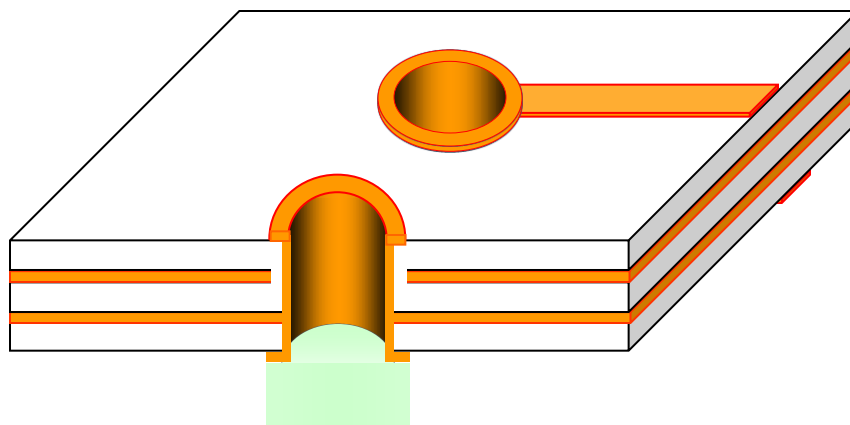
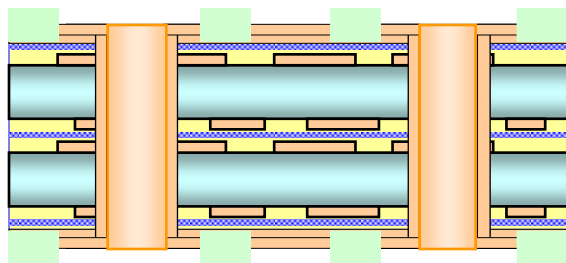
19. 外層顯影 Develop



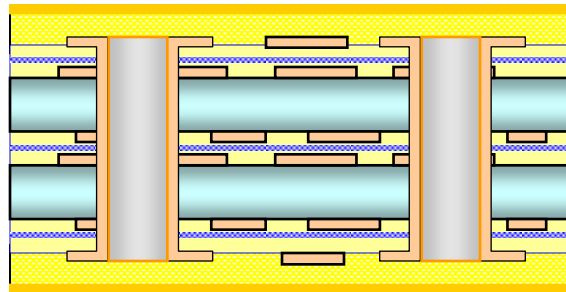
20. 蝕刻 Etch



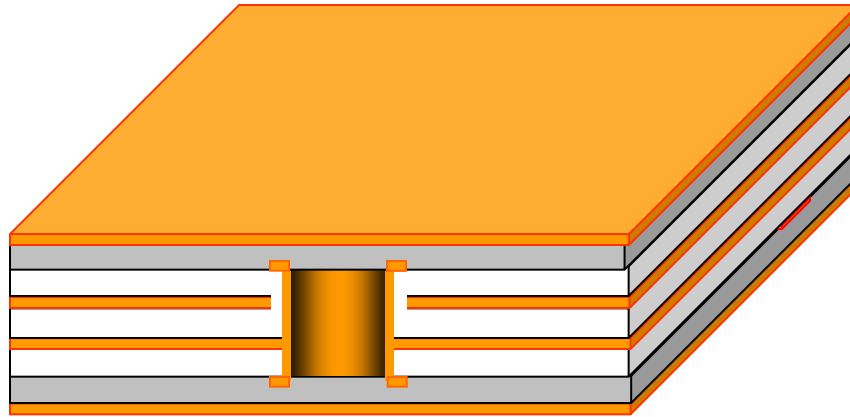
20. 去乾膜 Strip Resist



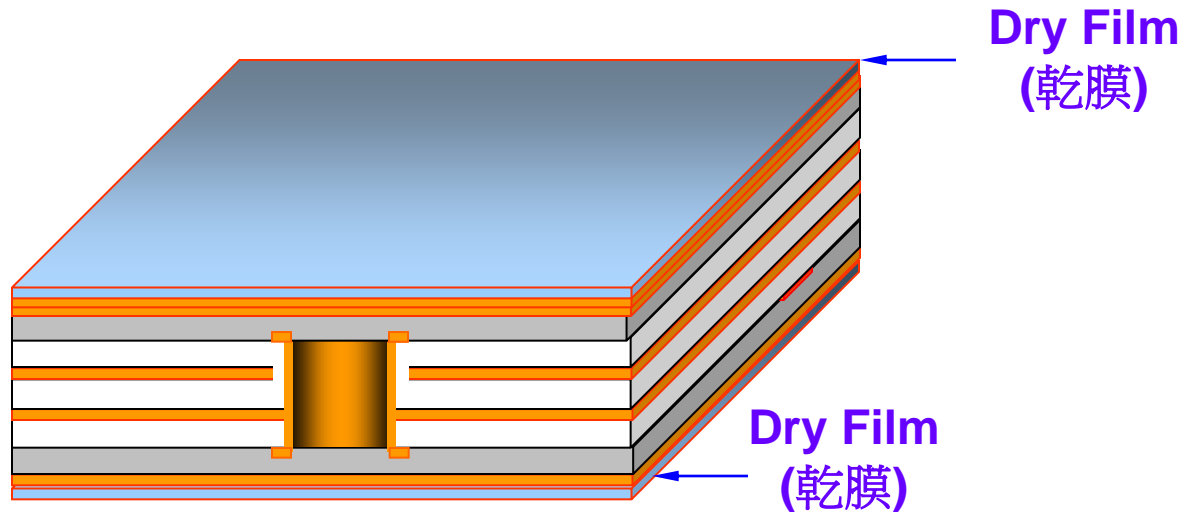
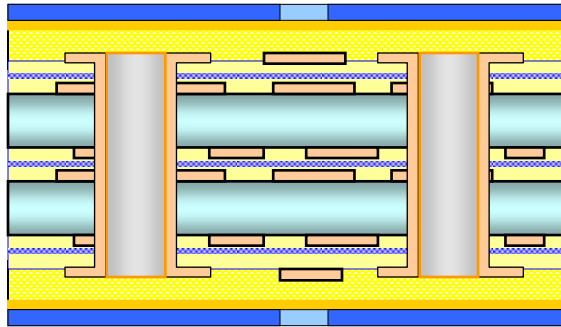
21. 壓合 (Build-up Layer Lamination)



RCC
(Resin Coated Copper foil)

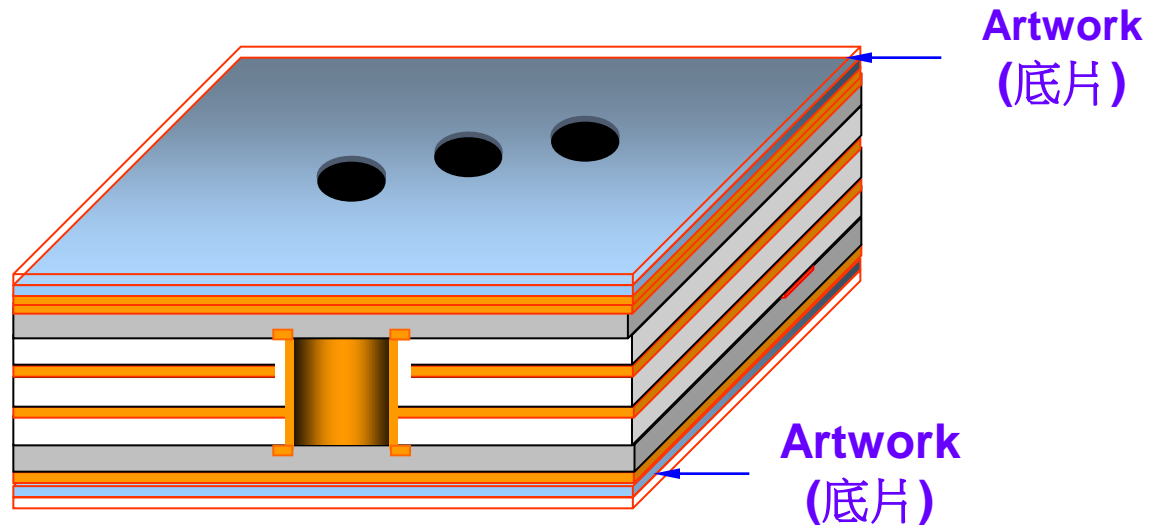


21. 護形層製作 (壓膜)(Conformal Mask)

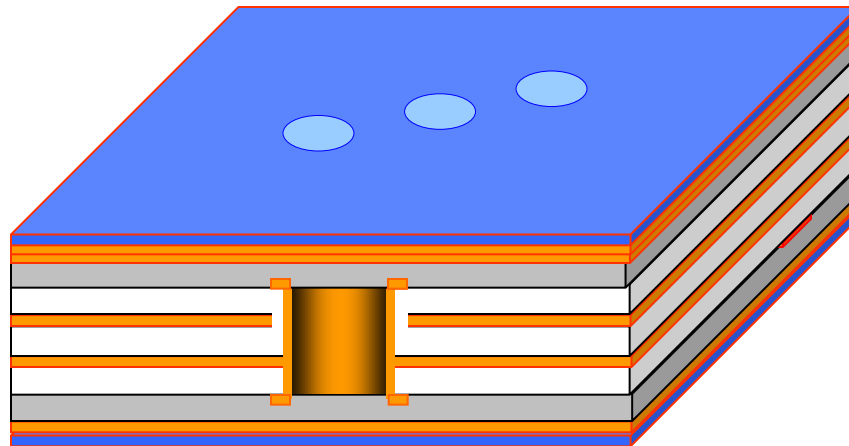


22. 護形層製作 (曝光)(Conformal Mask)

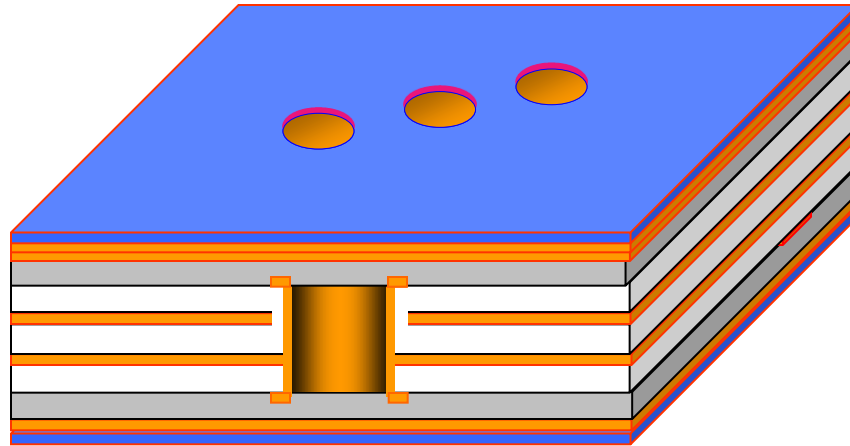
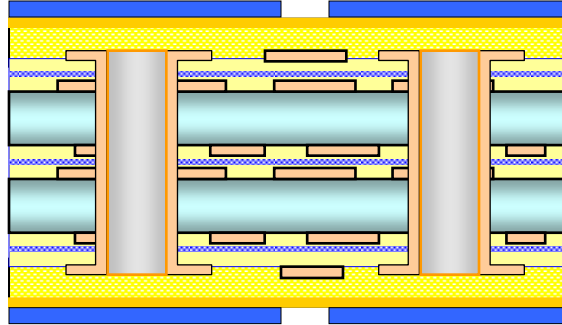
Before Exposure



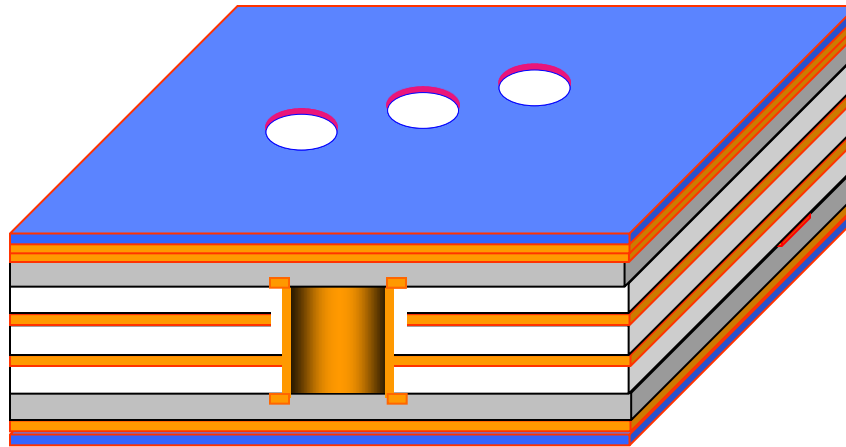
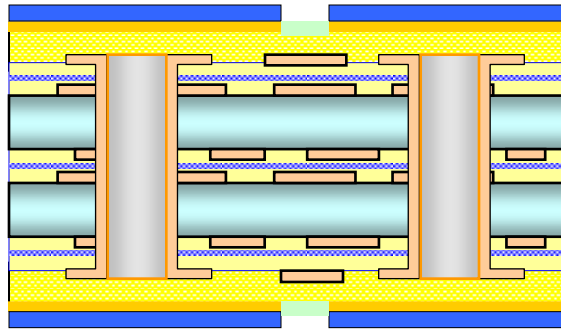
After Exposure



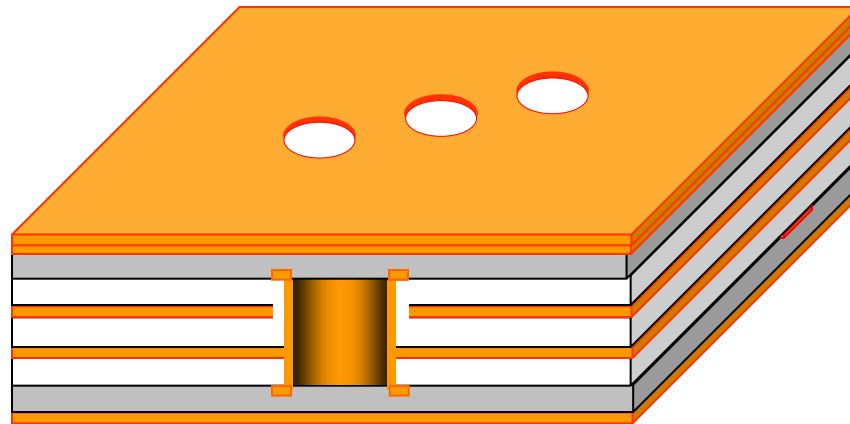
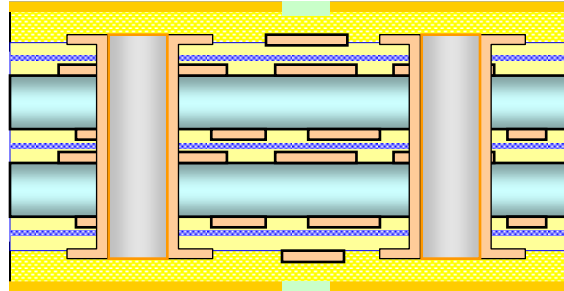
23.護形層製作 (顯像)(Conformal Mask)



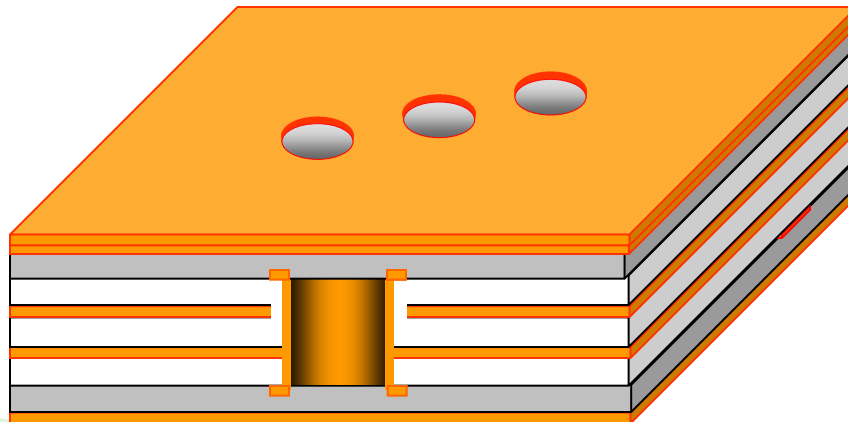
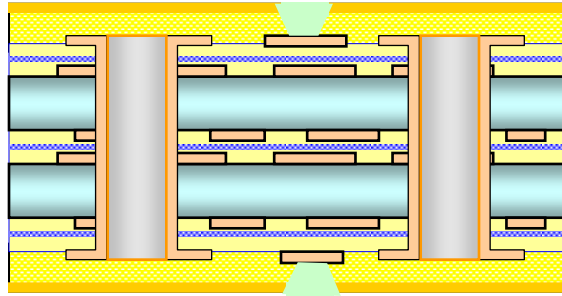
24. 護形層製作 (蝕銅) (Conformal Mask)



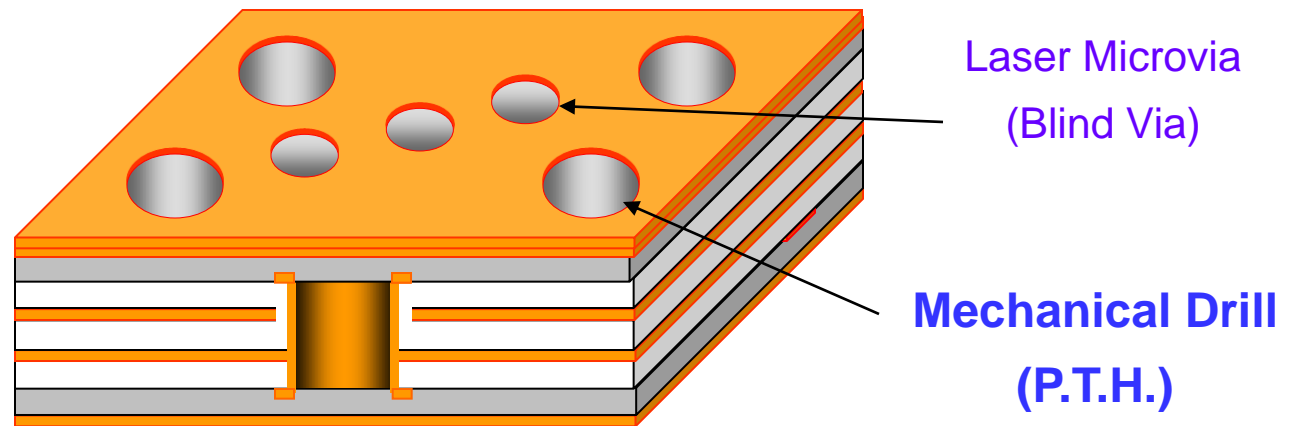
25. 護形層製作(去膜) (Conformal Mask)



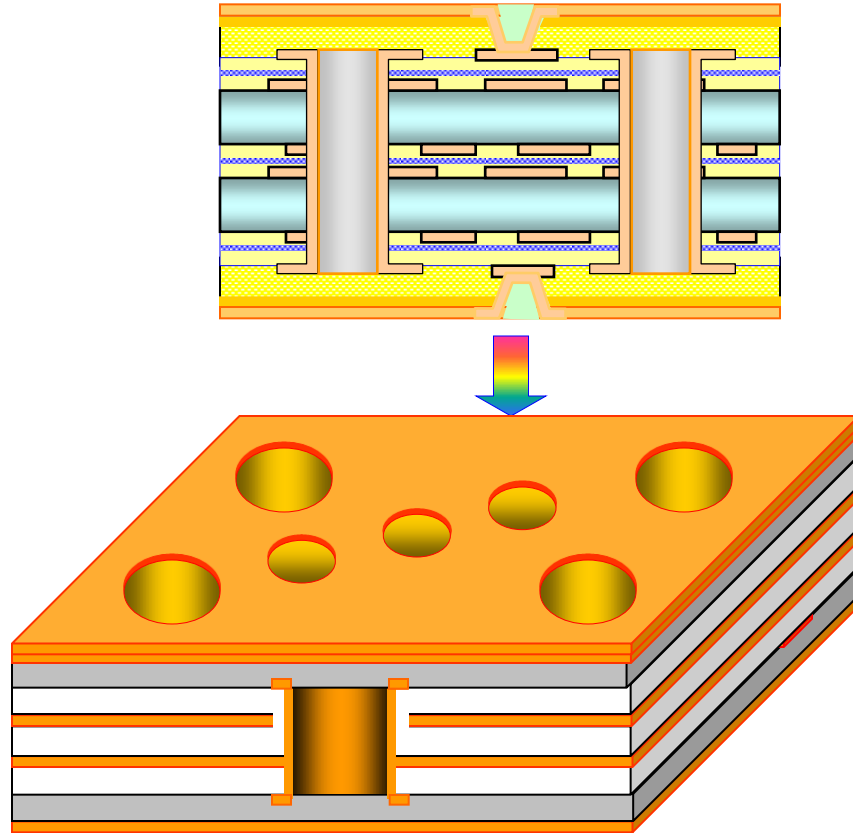
26. 雷射鑽孔 (Laser Ablation) 及機械鑽孔



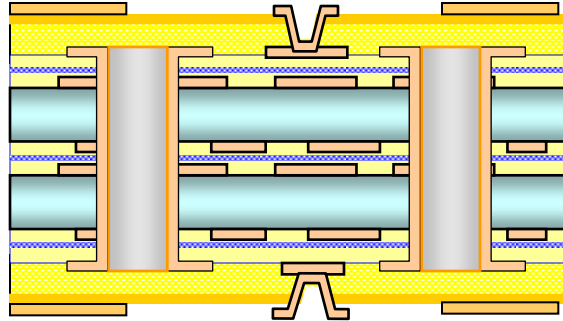
27. 機械鑽孔 (Mechanical Drill)



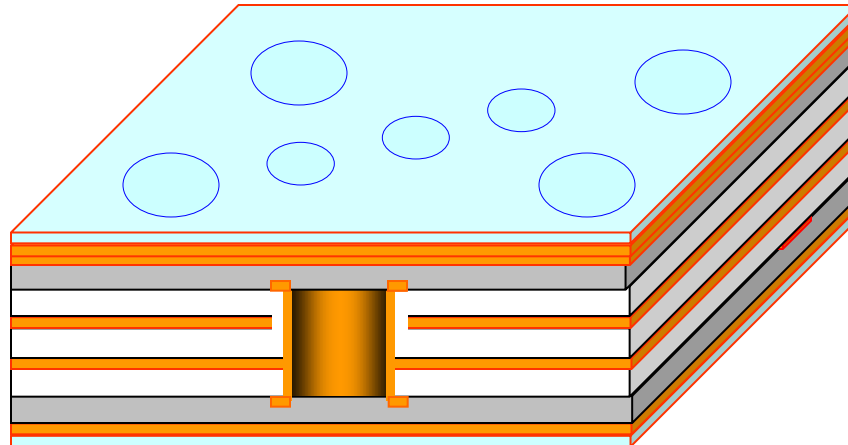
28. 電鍍(Desmear & Copper Deposition)



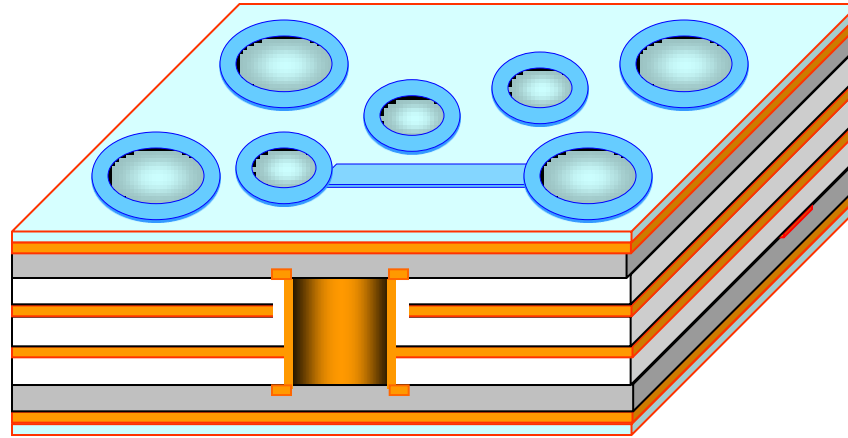
29. 外層線路製作 (Pattern imaging)



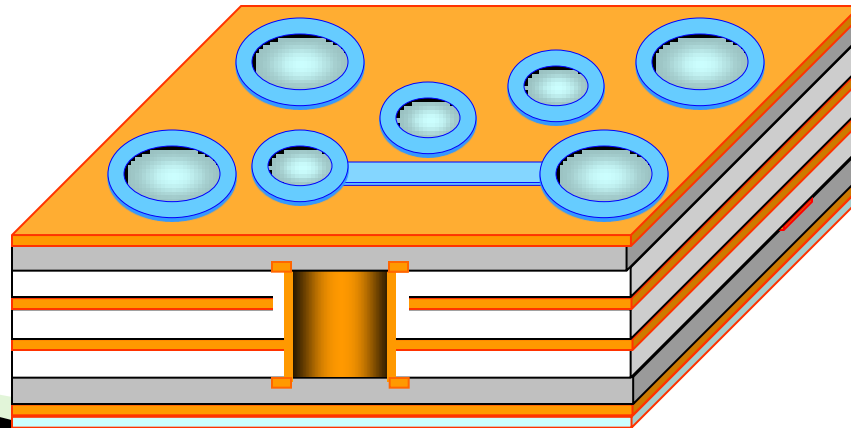
壓膜(D/F Lamination)



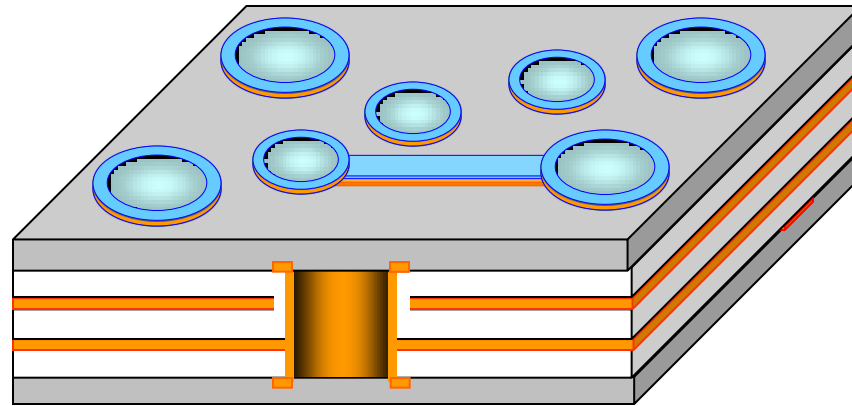
曝光(Exposure)



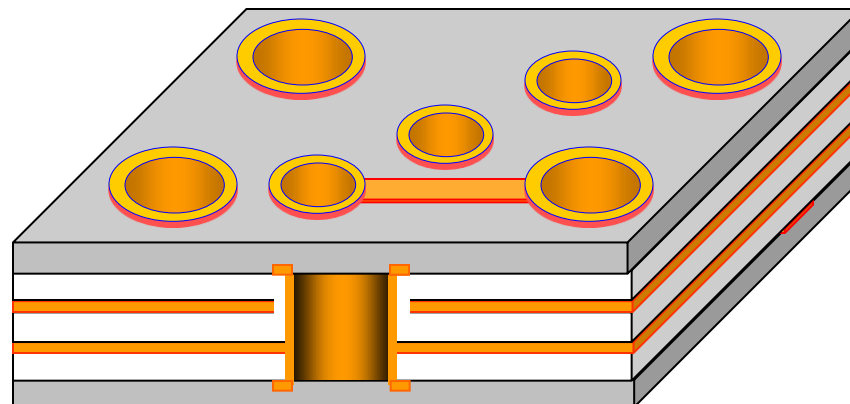
顯像(D/F Developing)



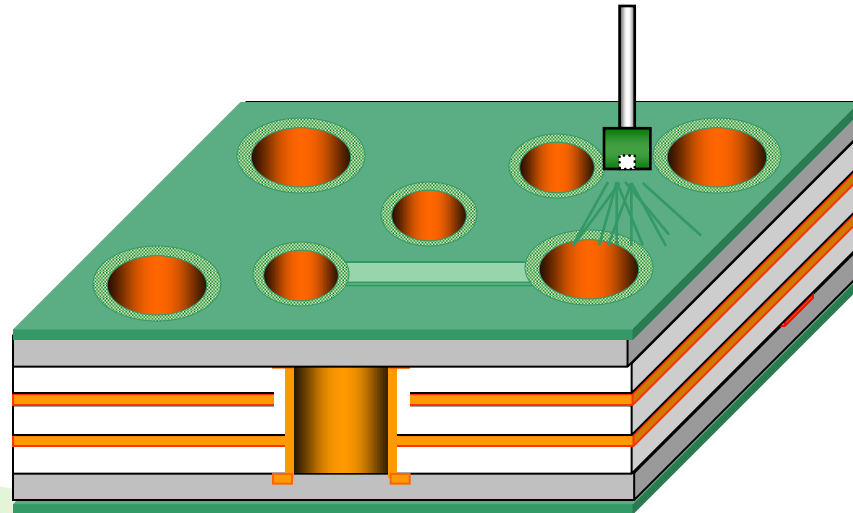
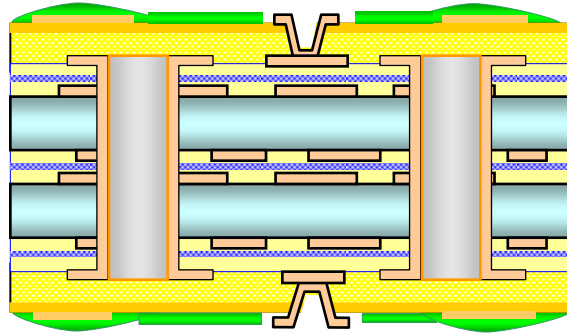
蝕銅 (Etching)



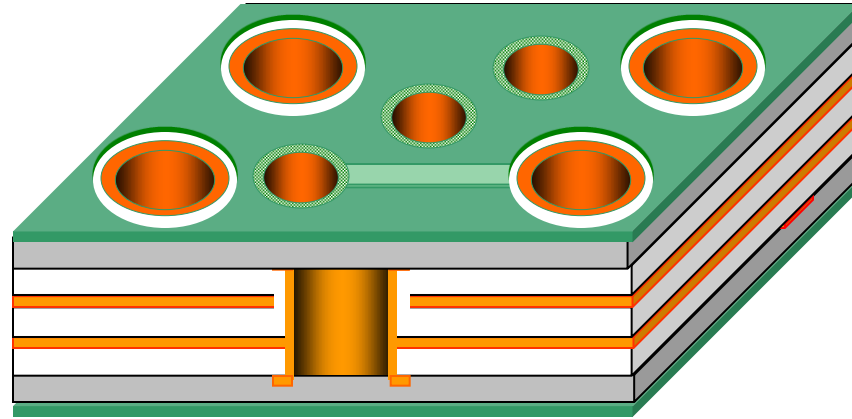
去膜 (D/F Stripping)



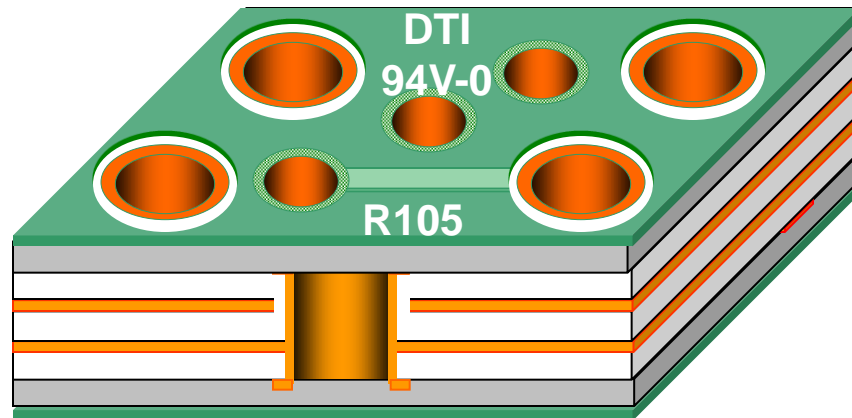
30. 防焊(綠漆)製作 (Solder Mask)



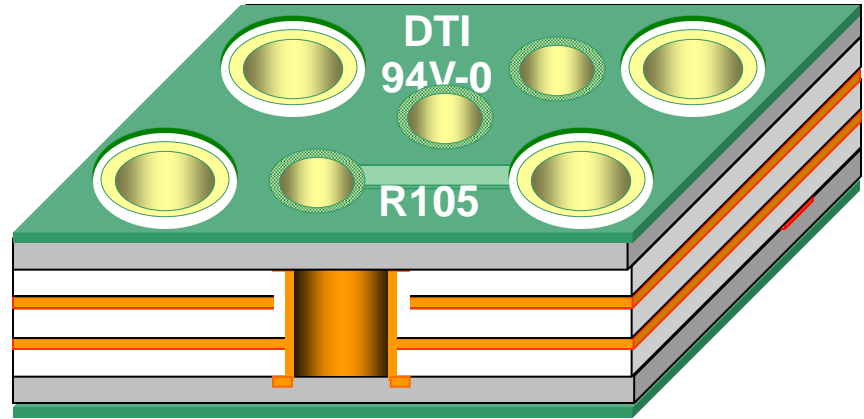
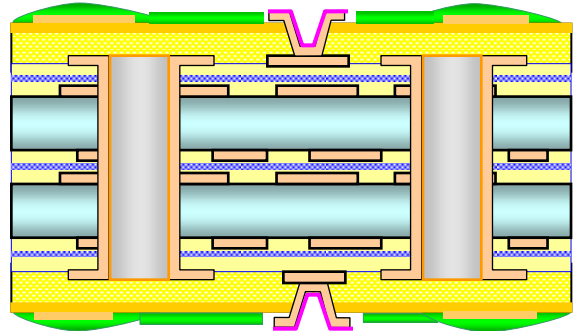
31. S/M 顯像 (S/M Developing)



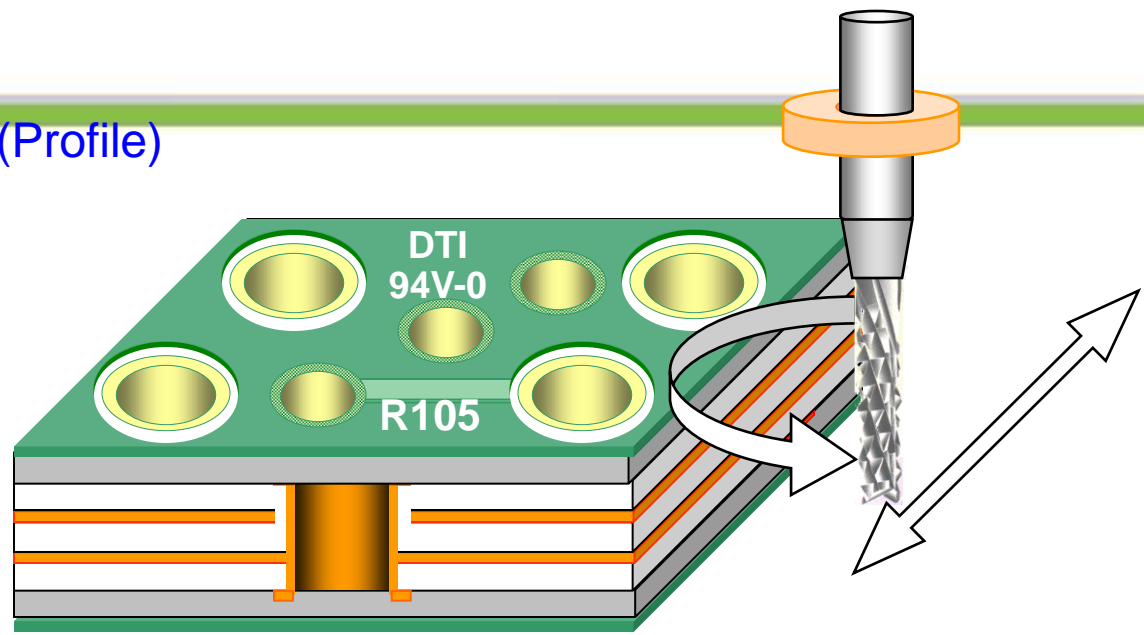
32. 印文字 (Legend Printing)



33. 浸金(噴錫.....)製作(Electroless Ni/Au , HAL.....)



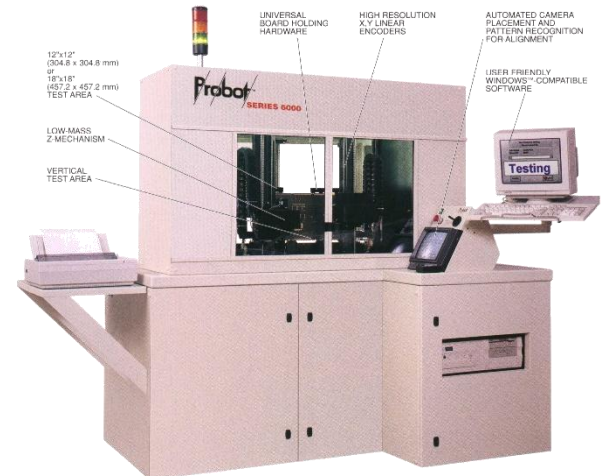
34. 成型 (Profile)



35. 測試 (Electrical Testing)

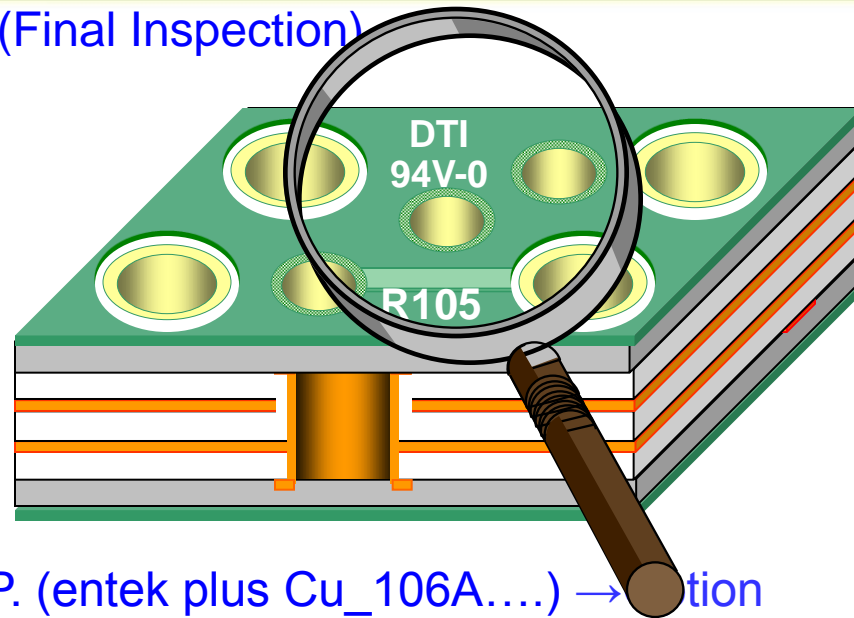


**Dedicate or universal
Tester**

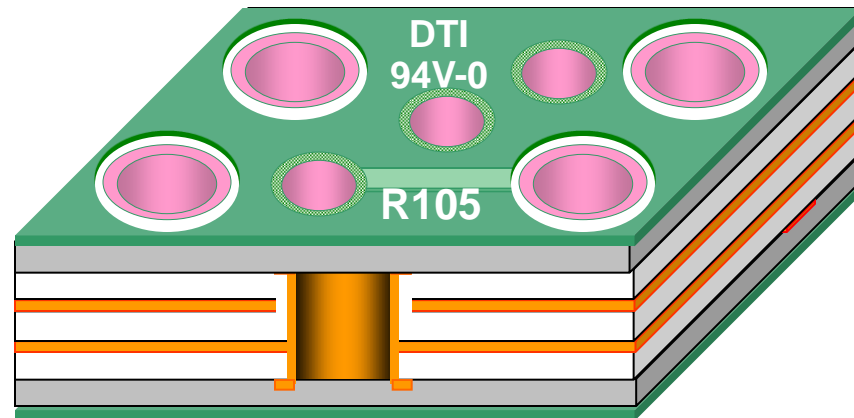


Flying Probe Tester

36. 終檢 (Final Inspection)



37. O.S.P. (entek plus Cu_106A....) → tion



Equipment

Photo

Equipment Photo

Exposure

AOI



Equipment Photo

Laser
Drilling



M/Drilling



Equipment Photo

X-Ray
Drilling



Cu Plating



Equipment Photo

CNC
Routing



SEC/EDS



Equipment Photo

IR

Thermal Shock



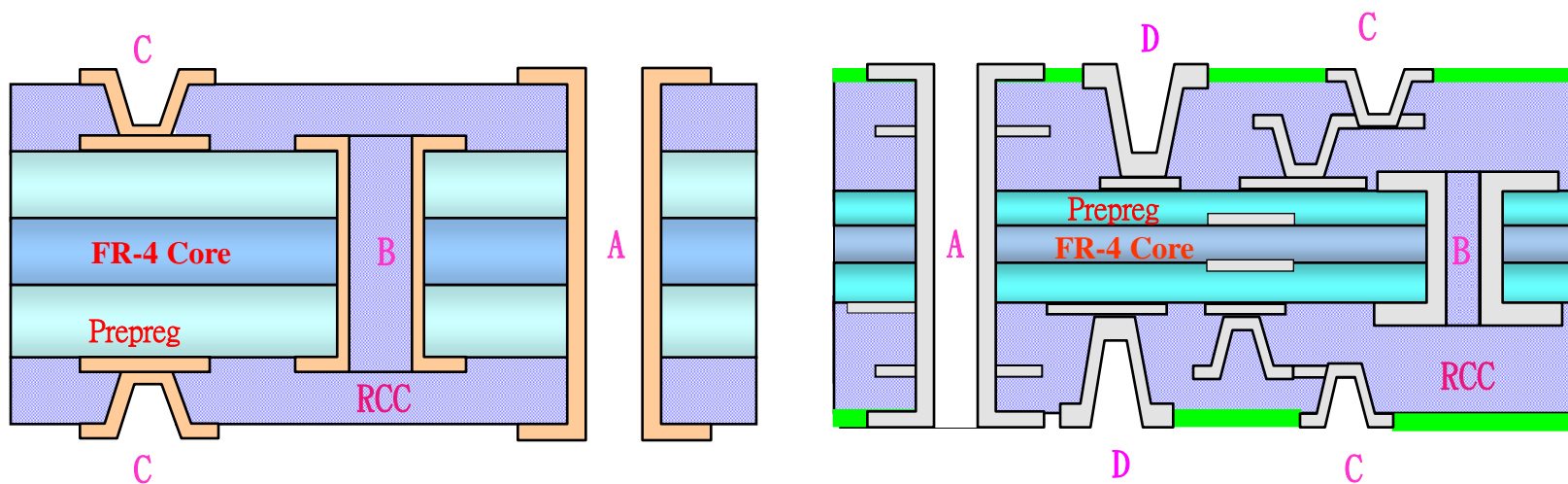


ROCKET
PCB

HDI Products

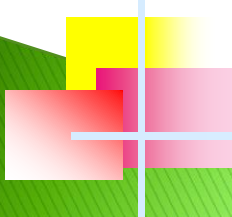
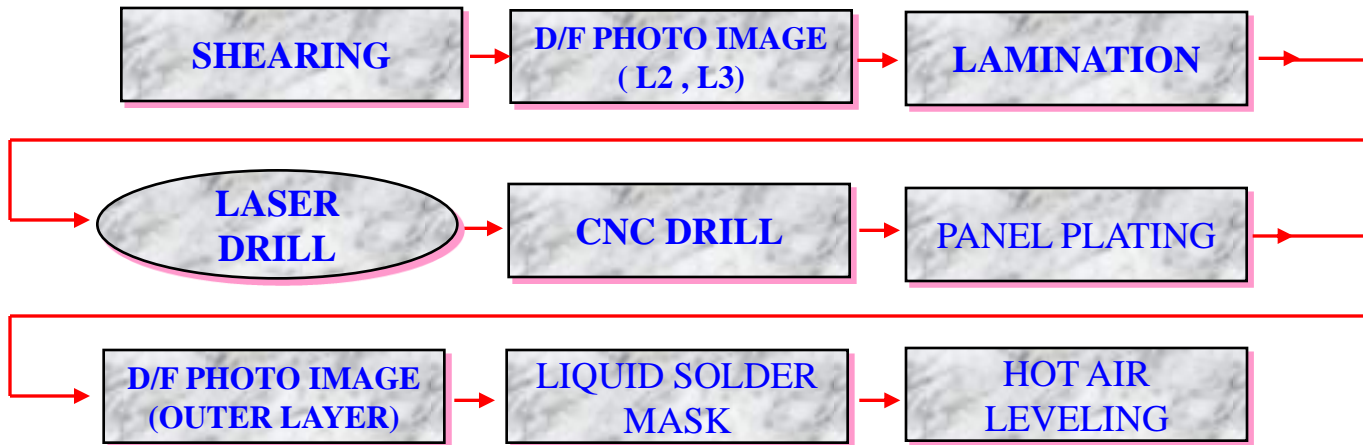
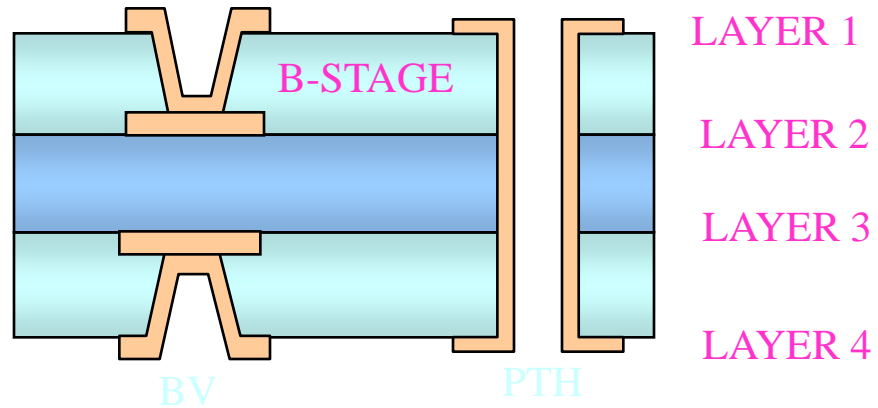
Buried Via and Laser Blind Via

- A = THROUGH Via Hole (導通孔)
- B = BURIED Via Hole (埋孔)
- C = STAGGER Blind Via (雷射盲孔)
- D = TWO LEVEL Laser Via (雷射盲孔)

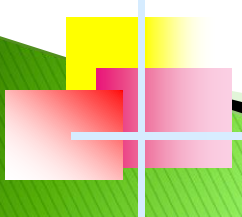
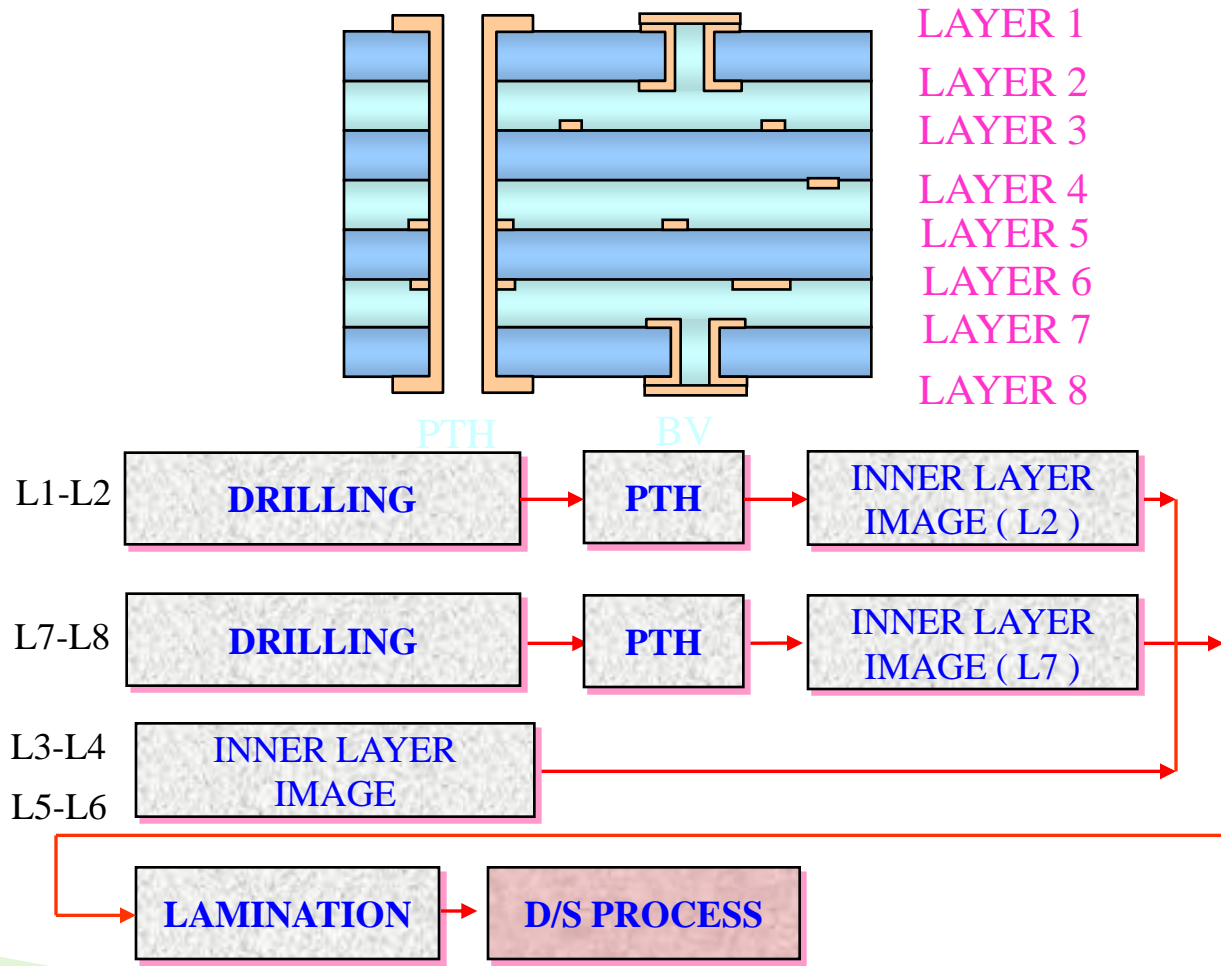


LASER BLIND & BURIED VIA LAY-UP

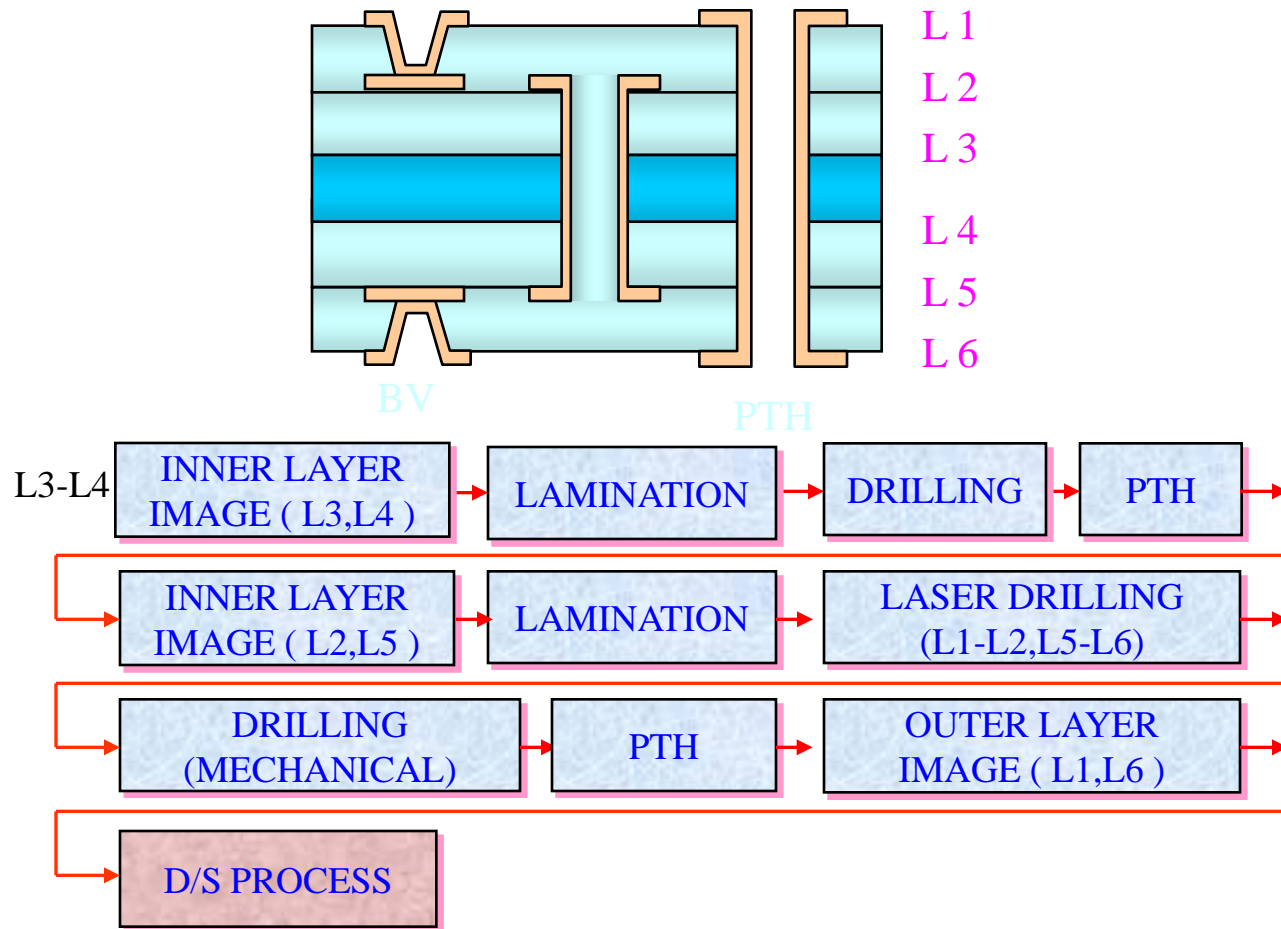
4Ls MLB with Blind Via Process



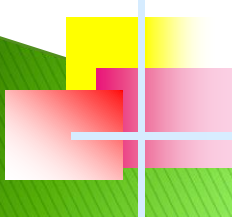
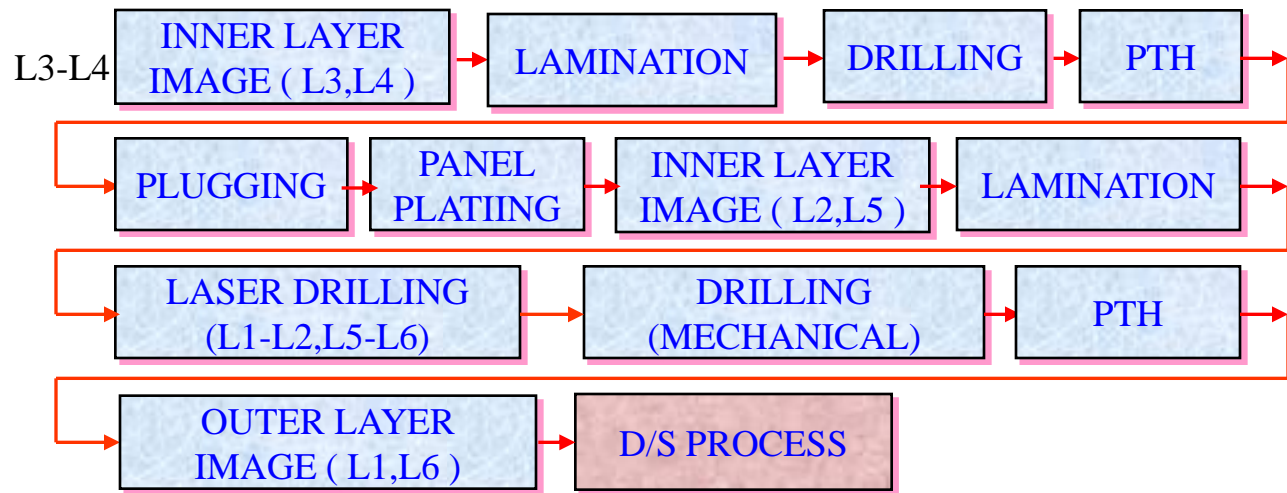
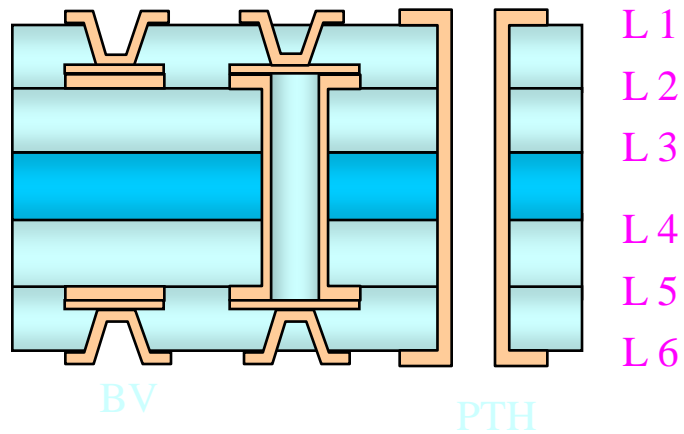
8Ls MLB with Blind Via Process



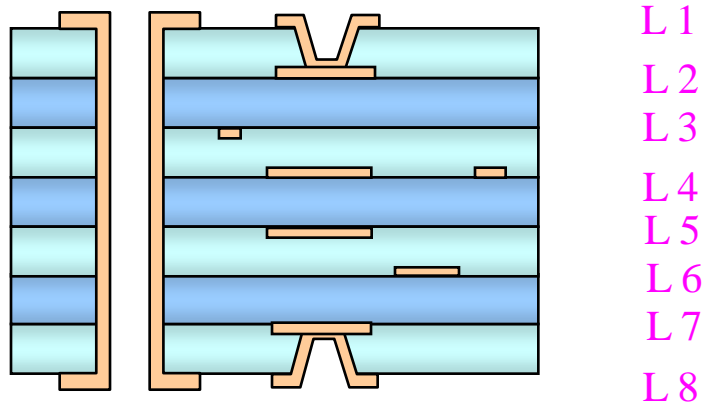
6Ls MLB with Blind & Buried Via Process



6Ls MLB with Blind & Buried Via Process

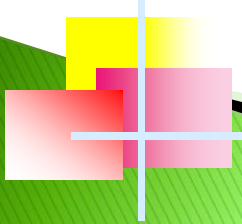


8Ls MLB with Laser Blind Via Process

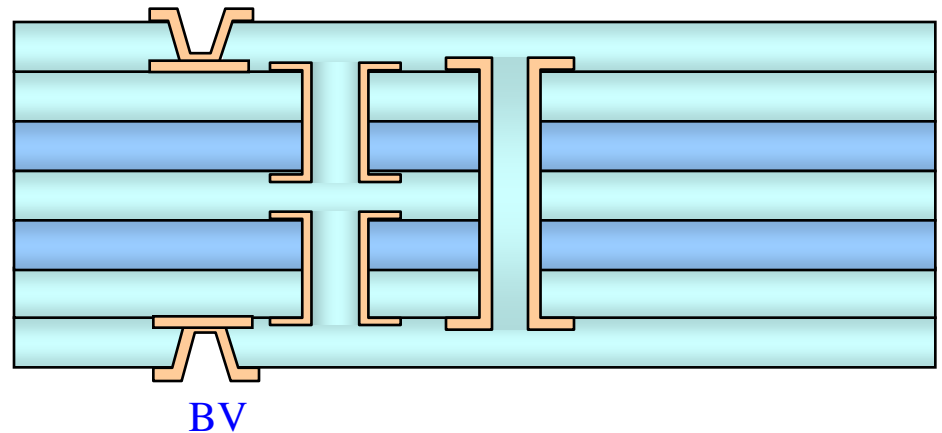


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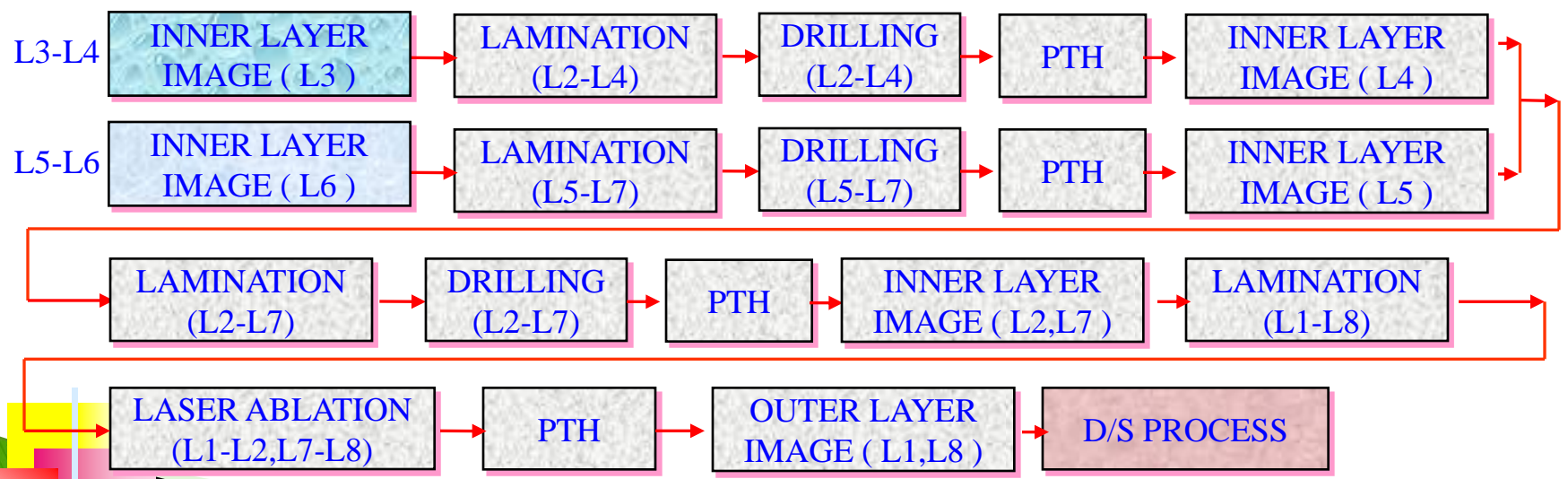
    graph TD
      A["L2-L3  
L4-L5  
L6-L7  
INNER LAYER  
IMAGE(L2-L7)"] --> B["LAMINATION  
(L1-18)"]
      B --> C["LASER DRILLING  
(L1-L2,L7-L8)"]
      C --> D["DRILLING (L1-L8)  
(MECHANICAL DRILL)"]
      D --> E["PTH"]
      E --> F["OUTER LAYER  
IMAGE (L1,L8)"]
      F --> G["AOI Inspection"]
      G --> H["Double Side  
PROCESS"]
  
```



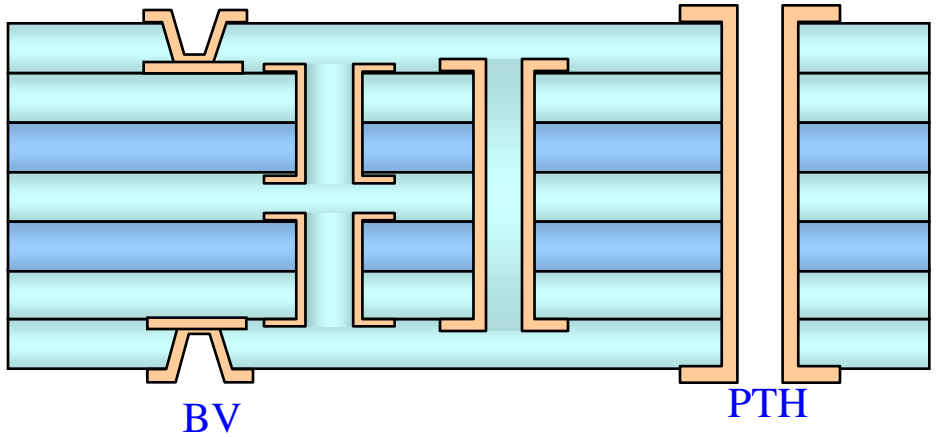
8Ls MLB with Laser Blind Via Process



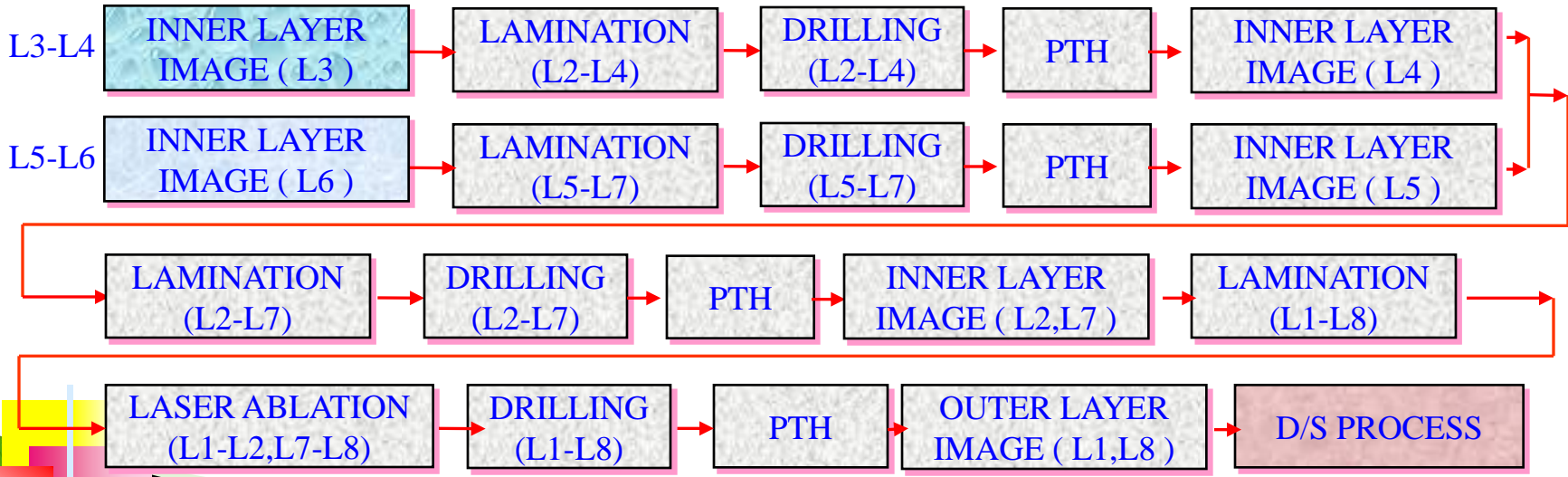
- LAYER 1
- LAYER 2
- LAYER 3
- LAYER 4
- LAYER 5
- LAYER 6
- LAYER 7
- LAYER 8



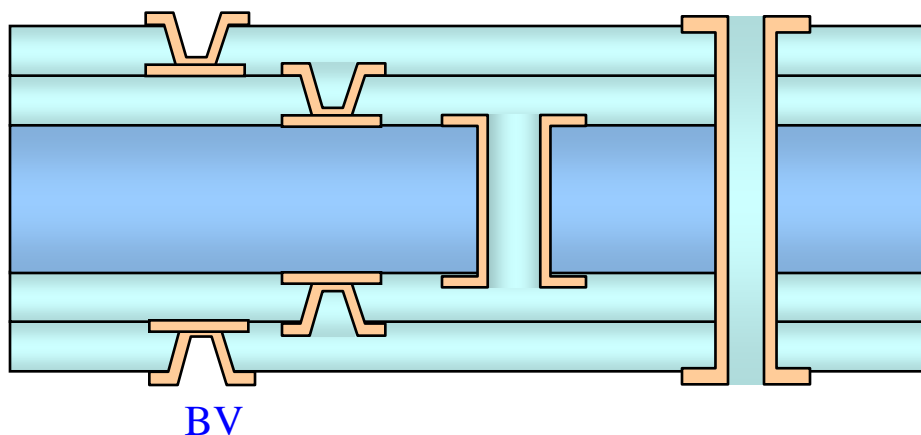
8Ls MLB with Laser Blind Via Process



- LAYER 1
- LAYER 2
- LAYER 3
- LAYER 4
- LAYER 5
- LAYER 6
- LAYER 7
- LAYER 8

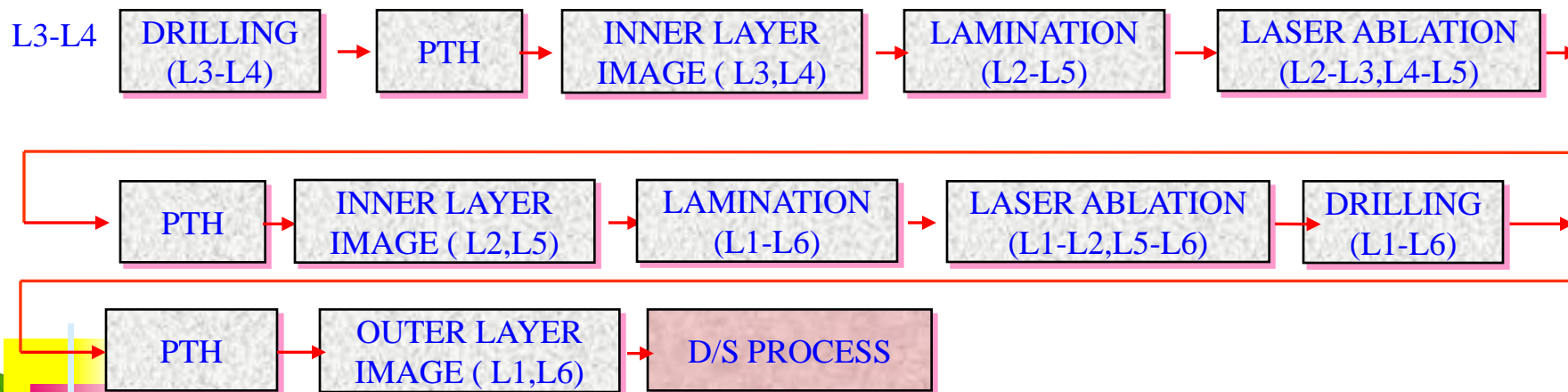


6Ls MLB with Laser Blind Via Process

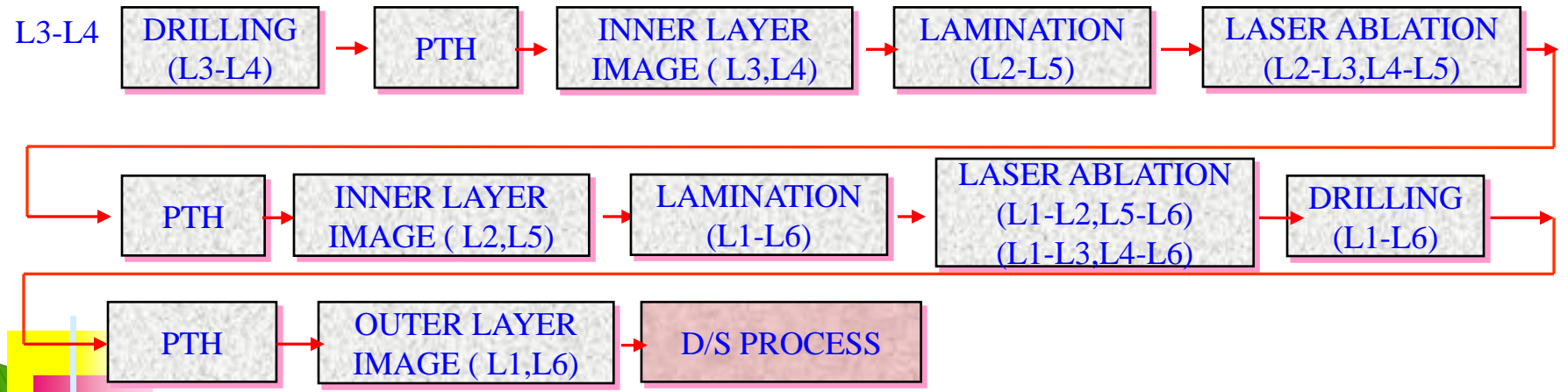
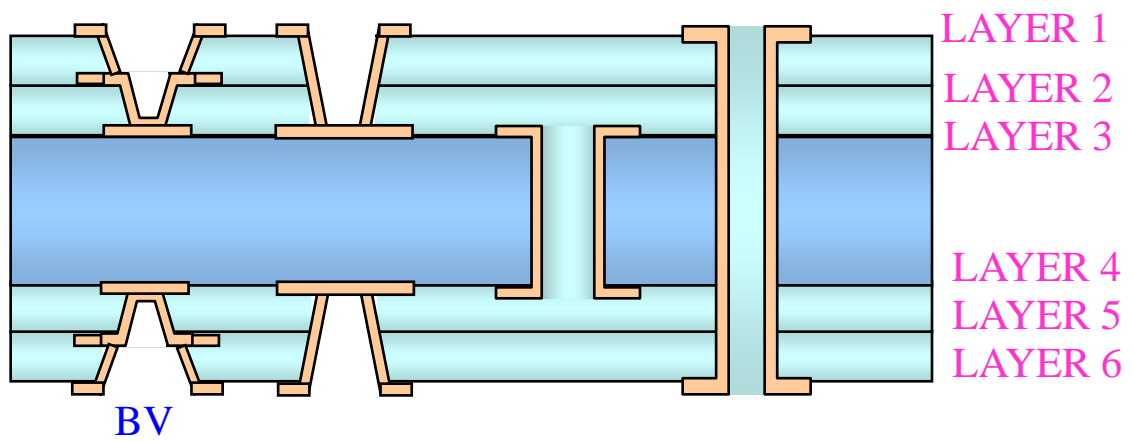


LAYER 1
LAYER 2
LAYER 3

LAYER 4
LAYER 5
LAYER 6



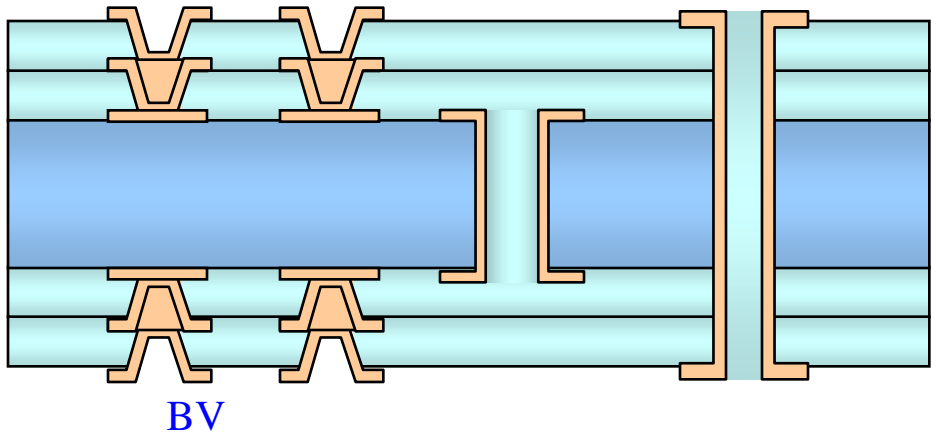
6Ls MLB with Laser Blind Via Process



6Ls MLB with Laser Blind Via Process

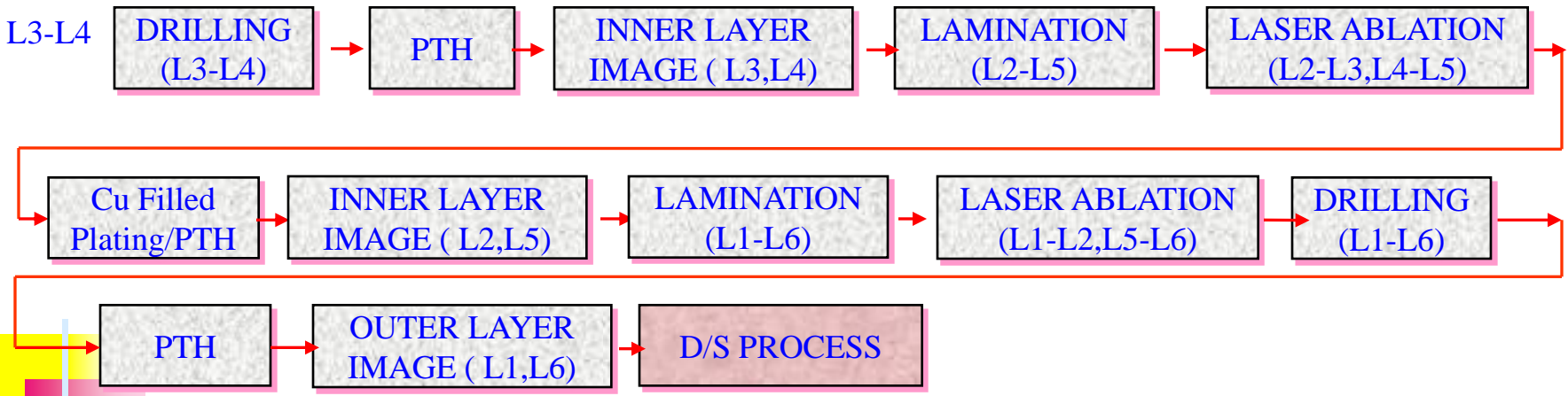


Developed



LAYER 1
LAYER 2
LAYER 3

LAYER 4
LAYER 5
LAYER 6

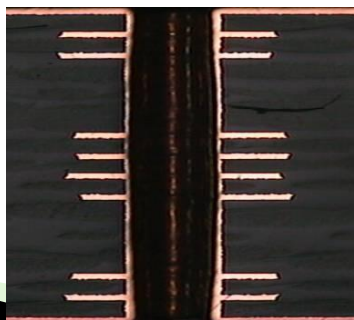


Technology Roadmap

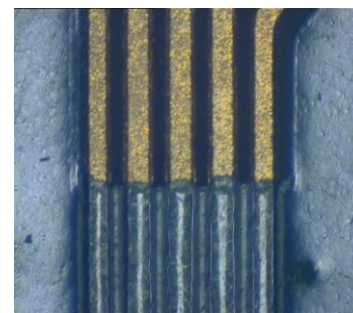
Technology Roadmap

| | 2005 | 2006 | 2007 | 2008 |
|----------------|--|--------------------------------------|--------|--------------|
| | PCMCIA 14 Layers | Blind Via HDI | | Buried C. R. |
| Line/Space | 4 / 4 mil | 3.5 / 3.5 mil | 3/3mil | 2.5/2.5 mil |
| Micro Via(D) | 5 mil | 4 mil | 3 mil | 2.5 mil |
| Surface Finish | Immersion Ni / Au Entek Selective Ni / Au | Gold Plating Immersion Silver&Tin | HASL | |
| Green Material | Halogen Free | Lead Free | | |
| Layer Reg. | 4 mil | 3.5 mil | 3 mil | 2.5 mil |

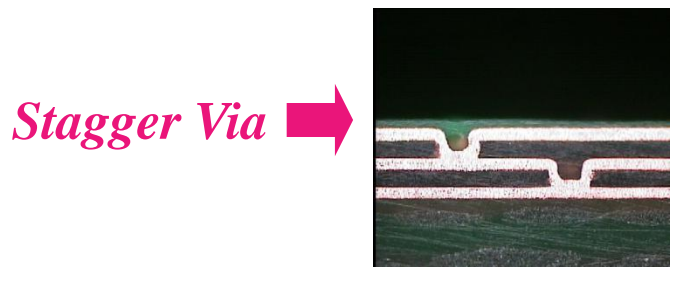
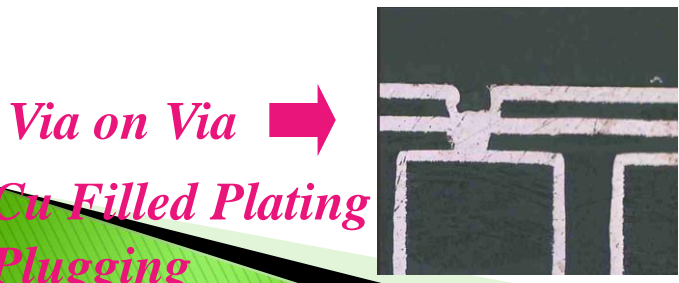
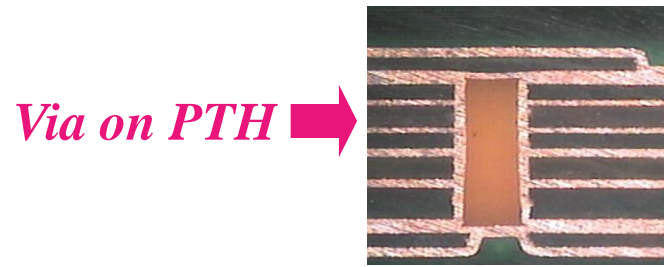
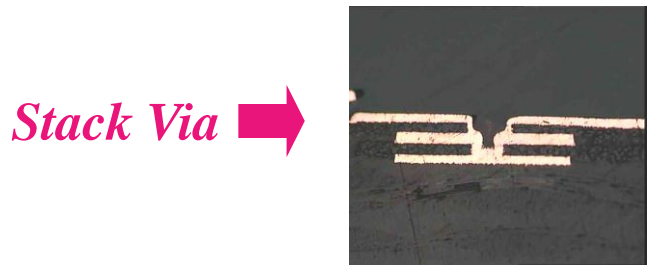
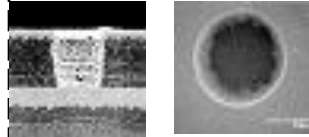
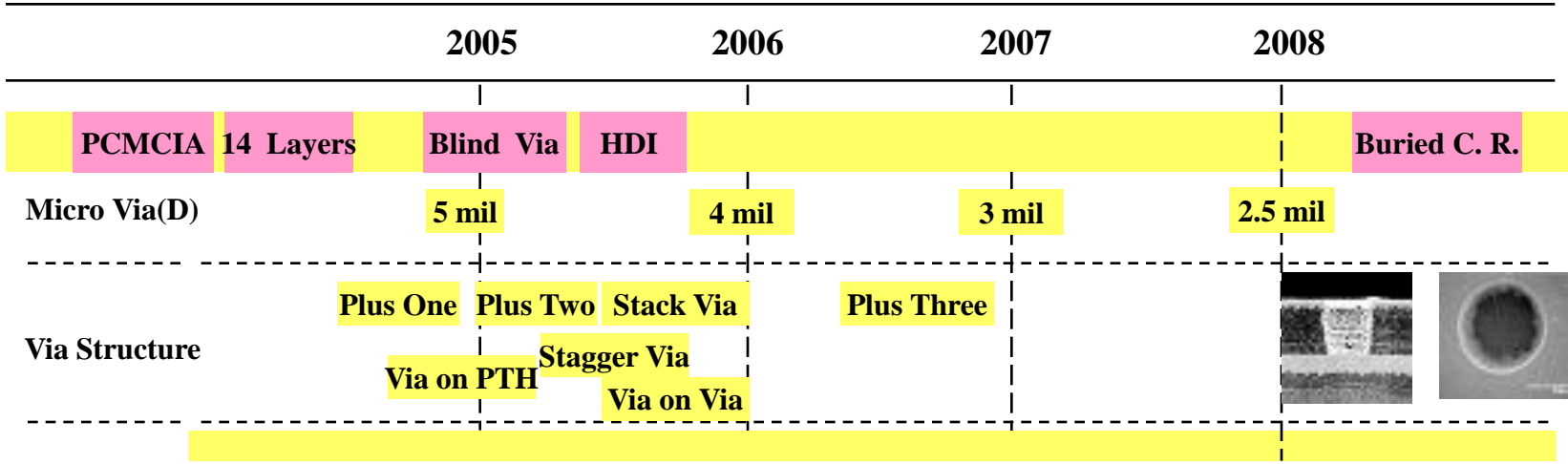
Layer Reg. →



Line/
Spacing. →



Technology Roadmap



- *Cu Filled Plating*
- *Plugging*

Capability (HDI)

| | | 2006 | 2007 | 2008 | 2009 |
|---|---------------|-------------|-------------|-------------|-------------|
| Max. build-up layer count per side | layers | 2 | 2 | 3 | 3 |
| Min. build-up dielectric thickness | mil | 2.6 | 2.6 | 2.0 | 2.0 |
| Min. micro via diameter (Unfinished) | mil | 5 | 4 | 4 | 3 |
| | mil | 12 | 12 | 10 | 10 |
| Max. micro via aspect ratio | | 0.8:1 | 0.8:1 | 0.9:1 | 1:1 |
| Line / Space | mil | 3/3 | 3/3 | 2.5/2.5 | 2/2 |
| Layer to layer Reg. Tolerance | mil | 3.5 | 3 | 2.5 | 2 |
| Solder Mask Reg. Tolerance | mil | 1.5 | 1.5 | 1.25 | 1 |
| Impedance control | % | <u>+10</u> | <u>+10</u> | <u>+7</u> | <u>+7</u> |
| Via on PTH | Yes/No | Yes | Yes | Yes | Yes |
| Via on Via | Yes/No | Yes | Yes | Yes | Yes |
| Plugged Plating | Yes/No | Yes | Yes | Yes | Yes |

Capability (PWB)

| | | 2006 | 2007 | 2008 | 2009 |
|--|------------|-------------|-------------|----------------|-------------|
| PTH Hole Size (Finished) | mil | 6 | 5 | 4 | 4 |
| Max. PTH aspect ratio | | 7:1 | 8:1 | 9:1 | 10:1 |
| Line / Space | mil | 3/3 | 3/3 | 2.5/2.5 | 2/2 |
| Min. SMT pitch | mil | 8 | 7 | 7 | 6 |
| Layer to layer Reg. Tolerance | mil | 3.5 | 3 | 2.5 | 2 |
| Solder Mask Reg. Tolerance | mil | 1.5 | 1.5 | 1.25 | 1 |
| Impedance control | % | ±10 | ±10 | ±7 | ±7 |
| Board flatness tolerance | % | 0.7 | 0.7 | 0.5 | 0.5 |
| Min. board thickness of 4 layers | mil | 14 | 12 | 12 | 10 |
| Min. board thickness of 8 layers | mil | 27 | 25 | 22 | 20 |
| Min. board thickness of 12 layers | mil | 41 | 37 | 34 | 32 |
| Max. board thickness | mil | 100 | 100 | 100 | 120 |

Thank you !